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Near-Equilibrium Chemical Vapor Deposition of High-Quality Single-Crystal Graphene Directly on Various Dielectric Substrates

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Graphene has attracted worldwide interest due to its distinctive band structure and fascinating physical properties, which have motivated the development of several efficient methods for the preparation of graphene, including mechanical cleavage,[1] epitaxial technique,[2] and chemical vapor deposition (CVD).[3,4] Among them, CVD on metal crystals is widely used in the large-scale synthesis of graphene films[3,4] and crystals,[5–9] and 5 mm single crystals of monolayer and bilayer graphene have been reported on copper.[10] However the graphene samples grown on metals need be transferred onto insulating materials for use in electronic devices, which results in loss of material, and furthermore it is difficult to avoid corrugation, contamination, and breakage of the graphene samples. The direct metal-catalyst-free growth of graphene on insulating substrates is thus important to the development of graphene nanoelectronics. Currently the growth of polycrystalline graphene films has been demonstrated on a variety of dielectric substrates such as sapphire, SiC, SiO_2, Si_3N_4 and BN,[11–16] which avoid the need for a complicated post-growth transfer process with its associated problems, showing their advantage compatible with current silicon processing techniques. However, these CVD processes have typically yielded polycrystalline graphene films composed of graphene grains with the lateral size smaller than 1 μm. The boundaries between graphene grains are expected to degrade the electrical and mechanical properties.[17–19] Therefore, it is highly desirable to prepare large-size single-crystal graphene directly on dielectric substrates to satisfy the applications of graphene in nanoelectronics.

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Recently, Yang, W. et al reported the epitaxial growth of nanometer-size single-domain graphene on hexagonal BN, and the growth approach opened new ways of graphene band engineering through epitaxy on different substrates.[20] Here we demonstrated that regular micrometer-size high-quality single-domain graphene can be directly grown on various dielectric substrates via a small-carbon-flow near-equilibrium chemical vapor deposition (CVD) process. The near-equilibrium CVD method allows C adatoms to reach the optional positions at the edge of graphene sheets with minimum energy to form stable crystalline phases with regular hexagonal and dodecagonal patterns. The maximum size of the graphene grains is about 11 μm, which is a factor of ~30 times larger than those previously reported on BN substrates.[20–22] The graphene grains show high crystalline quality with clean, wrinkle-free and breakage-free morphology, and a carrier mobility of greater than 5000 $cm^2 V^{-1} s^{-1}$. The ability to produce micrometer-size high-quality graphene grains directly on dielectric substrates is a step closer to real-world applications of graphene.

As described in Experimental section, the dielectric chips such as polycrystalline $Si_3N_4/SiO_2/Si$, SiO_2/Si and quartz, single-crystalline ST-cut quartz and sapphire with high melting points are utilized as growth substrates for graphene grains. The growth of graphene grains occur at about 1100 °C using CH_4 as carbon source, and the growth rate can be increased when improving temperature.[14,15] However, ultrahigh temperature is detrimental to some dielectric substrates. To grow large-size single-crystal graphene grains with a higher growth rate, a suitable growth temperature of about 1180 °C is thus used to realize our strategy.

Figures 1a and 1b show the atomic force microscopy (AFM) images of the $Si_3N_4/SiO_2/Si$ surface topography after growth. After exposure to the flowing reaction gas mixture (CH_4:H_2 = 2.3:50 standard cubic centimeters per minute (sccm)) for two hours, the surface of dielectric substrates became covered with graphene grains. These graphene grains with a uniform lateral size of ~400 nm, similar to single-domain graphene on BN substrate,[20–22] display a regular hexagonal shape in AFM height and phase images (Figures 1a,b). The thickness of these graphene grains on $Si_3N_4/SiO_2/Si$ substrate is about 0.73 nm (Figure 1a), which corresponds to the thickness of monolayer graphene. Regular graphene grains can also be grown on other dielectric substrates. The AFM images of the graphene grains directly grown on SiO_2/Si, quartz, ST-cut quartz and sapphire are shown in Figure 1c–f. These substrates have a flat surface

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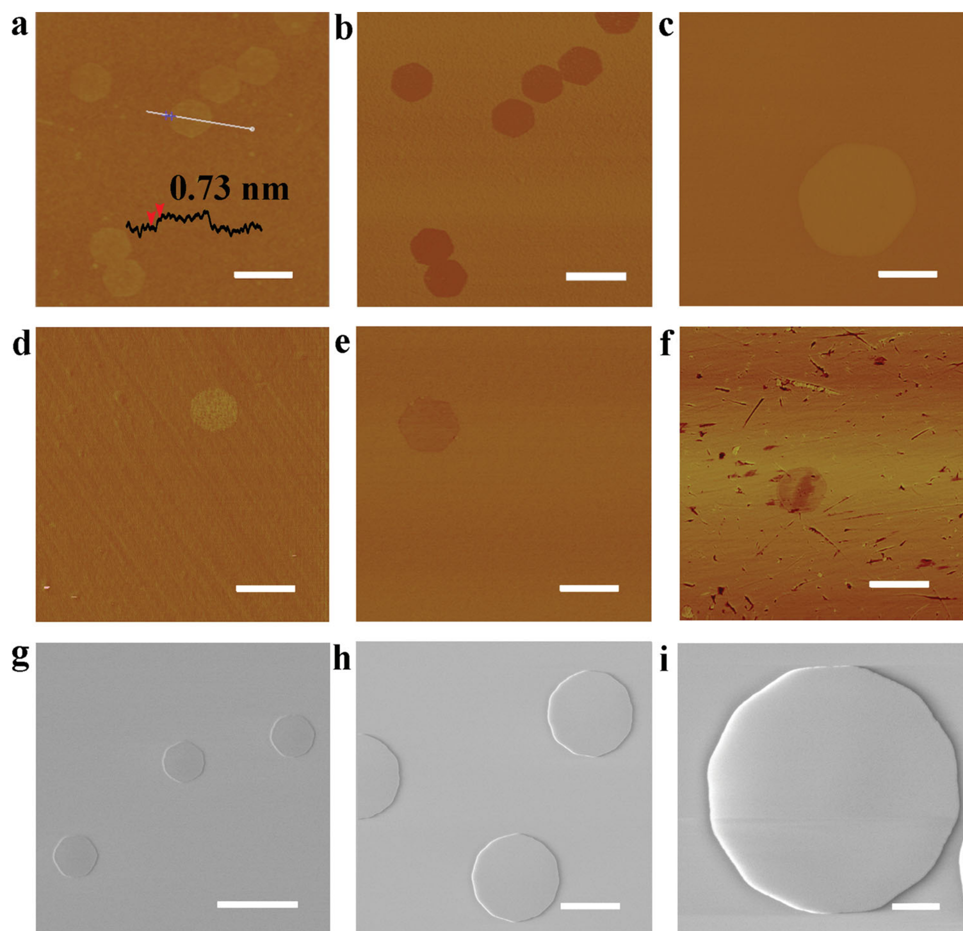

Figure 1. a) AFM height images of graphene grains on $Si_3N_4/SiO_2/Si$ substrate with a thickness of about 0.73 nm. Scale bar = 500 nm. b–f) AFM phase images of graphene grains on $Si_3N_4/SiO_2/Si$ substrate (b), SiO_2/Si substrate (c), quartz (d), sapphire (e) and ST-cut quartz (f). Scale bar = 500 nm. g–i) SEM images of graphene grains on SiO_2/Si substrates after different growth time. (g) 9 h, (h) 19 h, (i) 72 h. Scale bar = 2 μm. Nanoscale graphene grains have a hexagonal pattern while micrometer-size graphene grains have a dodecagonal pattern.

with a small surface roughness (Ra = 0.107 nm for sapphire; 0.174 nm for SiO_2/Si; 0.357 nm for ST-cut quartz; 0.380 nm for $Si_3N_4/SiO_2/Si$; 0.414 nm for quartz respectively) due to their high melting points and structural stability.[23–25] The growth of graphene grains directly on these substrates may have the same oxygen-aided growth mechanism (Supporting Information Figures S1 and S2) with a similar gowth speed,[14,15] and all graphene grains display the regular hexagonal shaped pattern. Recent experiments have reported the growth of graphene grains on metals, and used the regular hexagonal shape with edges parallel to specific crystallographic directions as evidence of the single-crystal nature of graphene.[5–9] In contract to metal crystals[5–9] and two-dimensional BN substrate,[20–22] these growth substrates used here have a complicated stereo network crystal structure similar to diamond. These results indicate that the growth of regular hexagonal single-crystal graphene is determined by equilibrium kinetics, and high-quality graphene grains could be grown on various substrates via a near-equilibrium CVD.

Figures 1g–i and Figure S3 show the typical scanning electron microscope (SEM) images of graphene grains with different lateral sizes. As the growth time increases from 9 h to 72 h at a flowing reaction gas mixture of CH_4 (1.9 sccm) and H_2 (50 sccm), the size of the graphene grains increases from ~1 μm to ~11 μm. These micrometer-size graphene grains display a uniform surface under SEM, and the thickness is about 1.0 nm measured by AFM (Figures S4 and S5), corresponding to monolayer graphene. Few-layer areas can be identified due to the different contrast under SEM (Figure S6). As seen from the SEM images (Figures 1i–h), the large-size single-layer graphene grains on dielectric substrates (Figure 1i) show an obvious apparent thickness compared with that of smaller graphene grains (Figures 1g, h). The morphology is different from those grown on conducting metals, but can be explained by the electron-beam-induced current on an insulator surface.[26]

Figure 2a shows the optical micrograph of graphene grains on a $Si_3N_4/SiO_2/Si$ substrate. Most graphene grains (pink) are monolayer graphene grains due to the slow self-limited growth, but there are nanosized risings on the surface of substrates, which also cause the growth of a small quantity of few-layer and multi-layer graphene grains (blue) on the surface.[14] Similar to that of transferred graphene samples on SiO_2/Si

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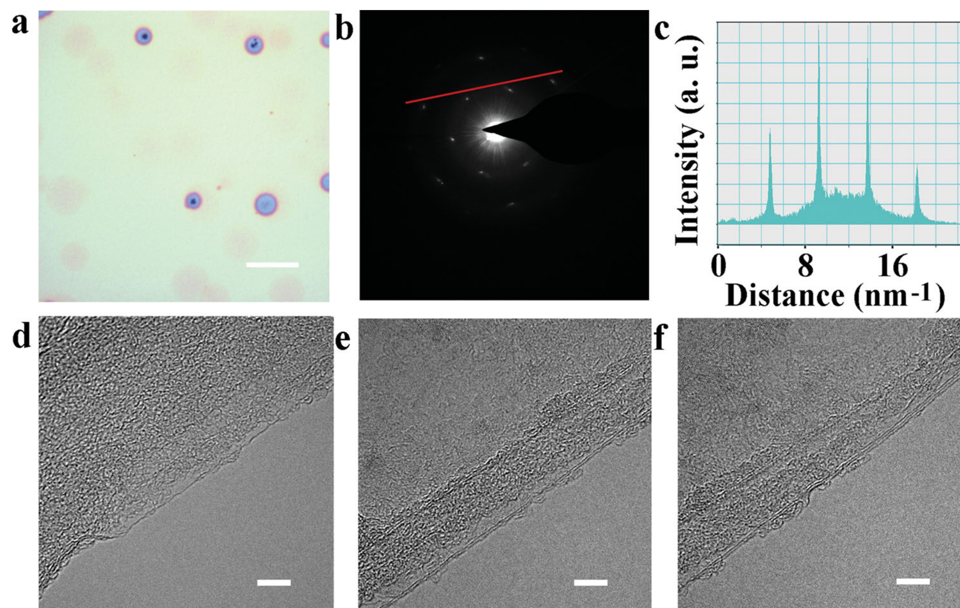

Figure 2. a) Optical micrograph of graphene grains on a $Si_3N_4/SiO_2/Si$ substrate. The optical image shows contrast indicative of predominantly monolayer grains (pink) with a small quantity of multi-layer graphene grains (blue). Scale bar = 10 µm. b) Hexagonal SAED pattern of the graphene grain. c) Diffracted intensity taken along the line in (b). The inner peaks are more intense than the outer ones, confirming that the region is monolayer. d–f) HRTEM images of monolayer (d), two-layer (e) and three-layer graphene (f). Scale bar 5 = nm.

substrates,[4,27] these micrometer-size graphene grains show a significant optical contrast on $Si_3N_4/SiO_2/Si$ substrate, which would make it straightforward to locate graphene for fabrication of graphene-based devices. The full XPS spectra of the $Si_3N_4/SiO_2/Si$ substrate and sapphire with discrete graphene grains on the surface have been shown in Figures S1 and S2. There were no other signals due to Fe, Co, Ni, Cu, or other metals,[28] indicative of the absence of metals in graphene growth. The characteristic XPS C 1s core-level spectrum (Figure S1a inset) was fitted with two peaks assigned as sp^2 carbon (284.8 eV) and C–H (285.3 eV). The C–H groups originate from H-terminated edges and the dominant peak is the sp^2 feature, confirming the graphitic structure of the as-grown grains.

The micro-structure of graphene grains was probed by using transmission electron microscopy (TEM) and selected area electron diffraction (SAED), which provided some important information about the quality of graphene grains. In Figures 2b–f and Figure S7, we showed the TEM images of graphene grains and its selected area electron diffraction (SAED) pattern. Differing from that of polycrystalline films,[14,15] only one set of six-fold symmetric diffraction spots (Figure 2b) was observed, indicating that the graphene grains have high-crystalline quality. The inner peaks are more intense than the outer ones, confirming that the region is monolayer (Figure 2c).[29] The layer count on the edges of high-resolution TEM images indicates the thickness of graphene grains, and the clear layer structure (Figures 2d–f) indicates that our graphene grains have the crystalline quality similar to that of metal-catalyzed graphene.[3,4]

The quality of graphene grains on dielectric substrates was further evaluated by using Raman mapping and spectroscopy with laser excitation at 514 nm. The mapping signals were extracted from the integrated intensities of the characteristic graphene Raman peaks, D (~1350 cm^{-1}), G (~1595 cm^{-1}), 2D (~2690 cm^{-1}), and their spatial dependences are plotted in **Figures 3**a–c for a single graphene grain on a $Si_3N_4/SiO_2/Si$ substrate and in Figures 3d–f for a single graphene grain on a SiO_2/Si substrate. As seen from the mapping signals of D peaks (Figures 3a, d), I_D is negligibly small, revealing that the graphene grain is almost defect-free, and the crystal quality is higher than that of polycrystalline graphene films.[14,15] I_{2D} is more than twice that of I_G, indicating that our samples are single layer graphene. The typical Raman spectra of the two graphene grains grown on $Si_3N_4/SiO_2/Si$ and SiO_2/Si substrates are shown in Figures 3g, h which display two characteristic peaks, corresponding to the G band and the 2D band respectively. The I_{2D}/I_G values of the graphene grains on $Si_3N_4/SiO_2/Si$ and SiO_2/Si are different due to the different substrates, while the full width at half-maximum (FWHM) of the 2D peaks are in substantial agreement (~31.3 cm^{-1} for graphene grains on $Si_3N_4/SiO_2/Si$, ~30.7 cm^{-1} for graphene grains on SiO_2/Si) with that of single-layer metal-catalyzed graphene.[3,4] The position, shape, FWHM of the 2D bands, together with I_{2D}/I_G and AFM thickness measurements (Figures S4 and S5), reveal that these graphene samples are single-layer graphene grains. Especially the Raman spectrum of graphene grains on SiO_2/Si substrates (Figure 3h) is in accord with that of metal-catalyzed graphene,[5–9] indicative of the high-quality of our graphene grains.

The CVD growth of graphene on dielectric substrates involves a vapor–solid–solid (VSS) growth mechanism. The growth law has suggested that the metal-catalyst-free growth is a surface deposition process with a very low reaction rate.[14] However the slow deposition just facilitates the control and the study of the growth of graphene grains on dielectric substrates.

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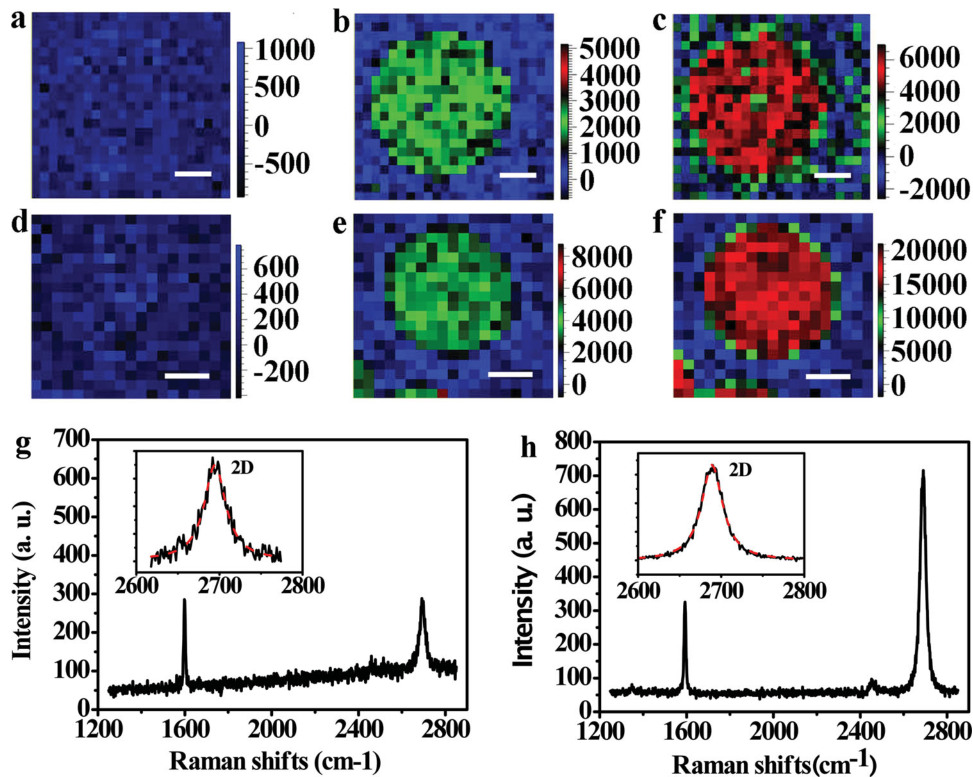

Figure 3. a–c) Raman mapping of a graphene grain grown on a $Si_3N_4/SiO_2/Si$ substrate. d–f) Raman mapping of a graphene grain grown on a SiO_2/Si substrate. (a,d) D peak. (b,e) G peak. (c, f) 2D peak. Scale bar = 2 µm. g) Typical Raman spectrum of the graphene grain on $Si_3N_4/SiO_2/Si$ substrate. h) Typical Raman spectrum of the graphene grain on SiO_2/Si substrate. The insets show the enlarged 2D peaks of the graphene grains with their fitted single Lorentzian curves.

After a near-equilibrium CVD of graphene on dielectric substrates, we have obtained two kinds of graphene grains with different morphologies—hexagonal and dodecagonal (Figure 1). According to previous reports, armchair (AC) graphene edge grows much faster than zigzag (ZZ) one, and the faster growing edges quickly disappear during CVD growth, and thus hexagonal graphene grains with ZZ edge are obtained on copper.[30,31] However, just the opposite, the shape of the graphene grains on dielectric substrates changes from hexagonal (Figure 1g) to dodecagonal (Figure 1i) with increasing size of the graphene grains. In contrast to CVD growth on metal surfaces, the diffusion of carbon on the surface of dielectric substrates is not expected to affect the evolution of the graphene shape due to the relatively higher diffusion barriers. The critical step in the growth is thus the reaction at the edges of newly-grown grains, which occurs with a frequency of $1/\tau$ between two successive events, where the distance that carbon atoms can travel along the edge within a time τ is $l_D = (2D\tau)^{1/2}$, and D is the diffusion constant along the edge. Thus for grains with side length L less than l_D, edge diffusion helps to reach an optimal shape of graphene with minimum energy, and the Wulff construction[32] can be used to determine the shape. Defining the energies for AC and ZZ forms as γ_A and γ_Z respectively, it has been suggested that when the condition[32]

$$\frac{\sqrt{3}}{2} < \frac{\gamma_A}{\gamma_Z} < \frac{2}{\sqrt{3}}. \tag{1}$$

is fulfilled, Wulff construction yields graphene edges consisting of both AC and ZZ edges. Outside of this range, either AC or ZZ edges will predominate. Our density functional theory calculations (Figure S8) predict γ_A/γ_Z = 1.14 and 1.32 eVÅ^{-1} for bare graphene edges, values which are reduced to 1.05 and 1.17 eVÅ^{-1} respectively, for hydrogenated edges on a SiO_2 substrate. Coupling to the SiO_2 substrate reduces the edge energies, and γ_A/γ_Z increases from 0.86 to 0.90, into the range covered by (1). Therefore, the redistribution of attached carbon atoms and reconstruction of graphene edges can more strongly affect the shape of graphene grains than suspended ones. The transition from hexagonal to a less anisotropic dodecagonal shape can be thus explained by the increase in the grain size L beyond l_D. A systematic study of the edge diffusion and the kinetics-limited growth dynamics is still ongoing.

To evaluate the electronic quality of the micrometer-size graphene grains, we have fabricated graphene FETs on $Si_3N_4/SiO_2/Si$ substrates ($Si_3N_4:SiO_2$ = 100:300 nm) and SiO_2/Si substrate (SiO_2 = 300 nm) by using an organic ribbon mask technique,[7,33] as described in **Figure 4**a and in Figure S9, and a SEM image of one FET on a $Si_3N_4/SiO_2/Si$ substrate is shown in Figure 4b. Figure 4c shows the typical output characteristics (drain current I_{DS} versus drain voltage V_{DS}) for the graphene device as measured under ambient conditions. The I_{DS} increases with increasingly negative gate voltage (V_G), in accordance with previous reports. Figure 4d shows the transfer curve (plot of I_{DS} versus V_G), and the positive Dirac point indicates that the grown

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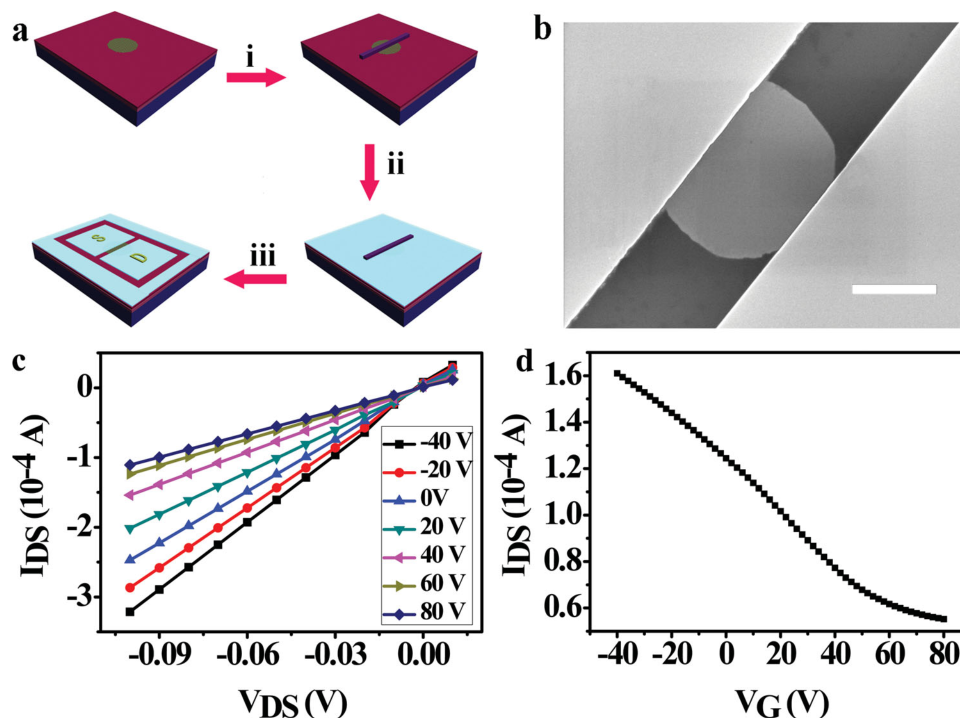

Figure 4. a) Schematic diagram of the ribbon technique for the preparation of graphene FETs. i, Place an organic ribbon on the surface of a graphene grain; ii, Deposit Pd film on the graphene surface by using the organic ribbon as a mark. iii, Remove the organic ribbon, and square off Pd film for the drain and source electrodes. b) SEM image of graphene grain FETs, Scale bar = 2 µm. c) Plots of drain current (I_{DS}) versus drain–source voltage (V_{DS}) recorded at different gate voltages. d) Transfer characteristics (plot of current (I_{DS}) versus gate voltage (V_G)) for the device at V_{DS} = 0.05 V.

graphene grain is p-type-doped from substrates.[34] The extracted mobility of devices on $Si_3N_4/SiO_2/Si$ substrates is better than that on SiO_2/Si substrate probably due to the different interaction between graphene and substrates (Figure S9).[15] The mobilities of the devices we studied on $Si_3N_4/SiO_2/Si$ substrates range from ~1300 to ~5650 $cm^2 V^{-1} s^{-1}$, which are better than those of metal-catalyst-free polycrystalline films,[11–16] and comparable to those of some metal-catalyzed graphene,[3–9] reflecting the high quality of our graphene lattice.

In summary, we realized the direct synthesis of large-size graphene grains on various dielectric substrates via a near-equilibrium CVD process. The maximum size can reach about 11 µm, which is a factor of ~30 times larger than those previously reported on BN substrates. These graphene grains display regular hexagonal and dodecagonal morphologies, and have high crystalline quality similar to that of metal-catalyzed graphene. The graphene grains give high carrier mobility when used in FET devices. Considering that inorganic materials, e.g., oxides, nitrides, sulfides, carbides and so on, are a large class of insulating materials, the ability to directly synthesize large-size high-quality graphene grains on dielectric substrates with a clean, wrinkle-free, and breakage-free morphology is important to basic research and practical applications.

Experimental Section

Preparation of Graphene: Graphene grains were directly grown on various dielectric substrates by using a small-carbon-flow but long-time-deposition method. The growth substrates, e.g. SiO_2/Si, $Si_3N_4/SiO_2/Si$, quartz, ST-cut quartz and sapphire, with their smooth surface faced down, were loaded into a horizontal silica tube mounted inside a high-temperature furnace. The furnace was heated to 1180 °C and stabilized for about 30 min at 250 standard cubic centimeters per minute (sccm) H_2 and 300 sccm Ar. Flowing reaction gas mixtures (CH_4:H_2 = 1.9~2.3:50 sccm) was used as the carbon source for the near-equilibrium growth of graphene. After a long reaction time, the methane supply was shut off and the system was cooled to room temperature under the flow of 50 sccm H_2.

Characterization: Atomic force microscopy (AFM) images were obtained using a NanoMan VS microscope in the tapping mode. Scanning electron microscopy (SEM) images were obtained using a Hitachi S-4800 scanning electron microscope. Transmission electron microscopy (TEM) was performed with Tecnai G2 F20 S-TWIN transmission electron microscope operated at 200 kV. Raman spectra were recorded at room temperature using a Renishaw inVia Raman Microscope with laser excitation at 514 nm, and mappings were taken over an extended range (1250–2850 cm^{-1}) with an exposure time of 1 s. X-ray photoelectron spectroscopy (XPS) was carried out on an ESCA Lab220I-XL spectrometer using an Al Kα X-rays as the excitation source. The base pressure was about 3 × 10^{-9} mbar, and the binding energies are referenced to the C 1s line at 284.8 eV.

Device and Electrical Measurements: FETs were fabricated on $Si_3N_4/SiO_2/Si$ and SiO_2/Si wafers by using the organic ribbon mask technique with Pd as source–drain electrodes and the doped silicon substrate as the back gate. Pd electrodes were fabricated on the graphene grains by thin-film evaporation. The electrodes had a thickness of 50 nm. The graphene devices were immersed in isopropyl alcohol for 10 h and annealed under vacuum at 120 °C for 3 h. The FET characteristics were measured in air at room temperature. A Keithley 4200SC semiconductor parameter analyzer was used to measure the electrical characteristics of the devices.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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