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Fabrication of graphene–silicon layered heterostructures by carbon penetration of silicon film

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Abstract

A new, easy, *in situ* technique for fabricating a two-dimensional graphene–silicon layered heterostructure has been developed to meet the demand for integration between graphene and silicon-based microelectronic technology. First, carbon atoms are stored in bulk iridium, and then silicon atoms are deposited onto the Ir(111) surface and annealed. With longer annealing times, the carbon atoms penetrate from the bulk iridium to the top of the silicon and eventually coalesce there into graphene islands. Atomically resolved scanning tunneling microscopy images, high-pass fast Fourier transform treatment and Raman spectroscopy demonstrate that the top graphene layer is intact and continuous, and beneath it is the silicon layer.

Keywords: two-dimension, layered heterostructures, graphene, silicon, STM

(Some figures may appear in colour only in the online journal)

Introduction

Ever since graphene was successfully exfoliated from graphite, it has been demonstrated to have unique electronic, optical and magnetic properties that have aroused considerable interest in the scientific and technological fields. Recently, graphene-based layered heterostructures and related two-dimensional (2D) materials [1–9], have been explored aggressively, allowing researchers to discover fascinating physical phenomena [10–13]. For instance, moiré superlattices arising in graphene coupled to hexagonal boron nitride provide a periodic modulation, enabling observation of a Hofstadter spectrum [14]. Graphene-based heterostructures have been used in electronic devices [11, 15], for example, a field-effect vertical tunneling transistor wherein two-dimensional tungsten disulphide serves as an atomically thin barrier between two layers of graphene [16].

Silicon, one of the most important semiconductor materials, is among the possible materials to be incorporated with graphene—hence the demand for integration between graphene and silicon-based microelectronic technology is substantial [12]. To realize a graphene–silicon heterostructure, on one hand, graphene must be layered on top of the silicon layer; moreover, in order to bring into play the unique properties of the graphene-based heterostructure, the interface between the graphene and silicon layers should be atomically smooth [17]. In the present work, we describe a new, easy and *in situ* technique to fabricate a two-dimensional graphene-silicon heterostructure by carbon penetrating a Si layer on an Ir(111) substrate.

One of the important mechanisms for growing graphene is segregation [18]. It requires that the metal substrate has relatively high carbon solubility. However, segregation can occur for metal substrates with relatively low bulk solubility, such as Ir [19, 20]. Thus, to begin our new method, the Ir(111) substrate was annealed at 1000 K in an ethylene (C_2H_4) atmosphere for 50 seconds, storing decomposed carbon atoms in the bulk iridium. Then we deposited silicon atoms on the Ir(111) surface and annealed the sample to 650 K, whereupon a well-ordered structure appeared. This structure was characterized as a $(2\sqrt{3} \times \sqrt{91})$ superstructure with respect to the substrate by means of low energy electron diffraction (LEED) and scanning tunneling microscopy (STM). With longer annealing times, carbon atoms or clusters were found on the surface, and they gradually coalesced into graphene islands. From atomic-resolution STM images of the graphene and from Raman spectroscopy, we confirmed that the graphene is intact and located on top of the silicon layer. Our experimental observations support the conclusion that a two-dimensional graphene–silicon heterostructure was fabricated successfully on Ir(111) substrate.

Methods and experiments

Our experiments were performed in an ultra-high vacuum (UHV) system with a base pressure about 2×10^{-10} mbar. The Ir(111) substrate was annealed at 1000 K in C_2H_4 atmosphere (3×10^{-5} mbar) for 50 s. This procedure may form graphene fragments, so the substrate was then etched over about ten layers by cycles of sputtering with argon ions (1×10^{-6} mbar for 30 s) and annealing until it yielded a distinct Ir (1×1) diffraction spot in a LEED pattern and clean surface terraces in STM images. Silicon atoms were deposited on Ir(111) at room temperature under UHV conditions from a piece of silicon (2 mm × 9 mm) heated by a direct current about 4 A. After a depositing time of 10 mins, the whole substrate was covered by as-deposited silicon atoms in STM measurements, and the deposited Si thickness was thus estimated as one monolayer. After deposition, the sample was annealed at 650 K for 30 mins for several cycles. To characterize its properties, we employed LEED to identify the heterostructure macroscopically and STM to image the surface in atomic scale detail. Raman spectra were acquired by a Renishaw spectrometer at 532 nm with 1 mW power.

Results and discussion

Figures 1(a)–(c) show a schematic of our unique new technique. First, the clean Ir(111) substrate with carbon atoms dissolved inside was prepared (see figure 1(a)); then, after silicon deposition and subsequent annealing, an ordered silicon superstructure appeared on the Ir(111) surface, as shown in figure 1(b); as annealing continues, the carbon atoms stored in the bulk iridium penetrate to the top, and eventually coalesce into graphene islands on top of the silicon layer (figure 1(c)). Thus, a graphene–silicon heterostructure has been fabricated on Ir(111) surface by a new and easy technique—pumping carbon atoms from underneath silicon film.

The structure of the heterostructure grown on Ir(111) surface was characterized by the arising LEED pattern macroscopically and by the corresponding STM images. In figure 1(d), the six bright spots indicated by the blue arrow can easily be assigned to the Ir(111) substrate with six-fold symmetry. The corresponding STM image in figure 1(g) shows clean surface terraces. After the preparation of the substrate, we deposited silicon atoms onto the Ir(111) surface. At room temperature, silicon atoms did not form any ordered structures; they aggregated as dispersed clusters on the surface, as we observed in STM images (not shown here). After annealing at 650 K, a new superstructure emerged, as was confirmed by a LEED pattern, as shown in figure 1(e). In addition to the diffraction spots from Ir(111) [21], a group of new spots appeared, indicating the formation of a well-ordered structure probably consisting of silicon. To verify this, we further employed STM to observe the annealed sample. As seen in figure 1(h), with the increased substrate temperature, the disordered silicon clusters disappeared, and instead, the entire surface was carpeted with a long-range ordered superstructure. Considering the LEED pattern together with the STM image, the silicon superstructure can be determined to be a $(2\sqrt{3} \times \sqrt{91})$ superstructure with respect to the Ir(111) substrate.

Next, we annealed the sample at 650 K for several cycles. Another six diffraction spots emerged in the LEED pattern, as shown in figure 1(f). In order to make it clear, we enlarged parts of the diffraction spots in the bottom-left corner of the picture, denoted by the yellow circle. Comparing their reciprocal lattice with the Ir(111) lattice [21, 22], we speculated that these spots could be ascribed to the graphene lattice. This assumption was confirmed by STM imaging. In figure 1(i), a graphene island is located on top of the silicon layer. Similar graphene islands can be seen widespread in different scanning areas on the sample surface, which is consistent with the LEED pattern. In the process of the two-dimensional heterostructure formation, it is noteworthy how graphene islands formed on top of the silicon layer. In the first step, we had stored carbon atoms in the bulk iridium. Thus, we thought that, with longer annealing times, the carbon atoms penetrated from the bulk iridium to the top of the silicon layer and eventually coalesced into graphene islands.

In order to verify this speculation, we scanned the sample after each annealing cycle. Fortunately, we observed the evolution of the graphene islands, as shown in figure 2. After the first annealing cycle, we scanned a small area, as seen in figure 2(a), which shows the extreme flatness of the long-range ordered silicon superstructure. We also noted other bright spots located on top of the silicon layer, which we supposed to be carbon atoms and clusters. Then we enlarged the scanning region, and we found that the bright spots arranged themselves regularly on the silicon layer, as shown in figure 2(b). These bright spots could be pure carbon or SiC clusters. However, our experimental temperature (below 650 K) was not high enough to form SiC (above 870 K, according to the previous report [23]). Thus we can conclude that at the beginning of annealing, some carbon atoms penetrated from the Ir substrate to the top of the silicon layer.

Then, after annealing the sample for two more cycles, small graphene islands emerged on top of the silicon layer, as shown in figure 2(c). Note that there are, at this point, much larger graphene islands in the middle of the STM image, and

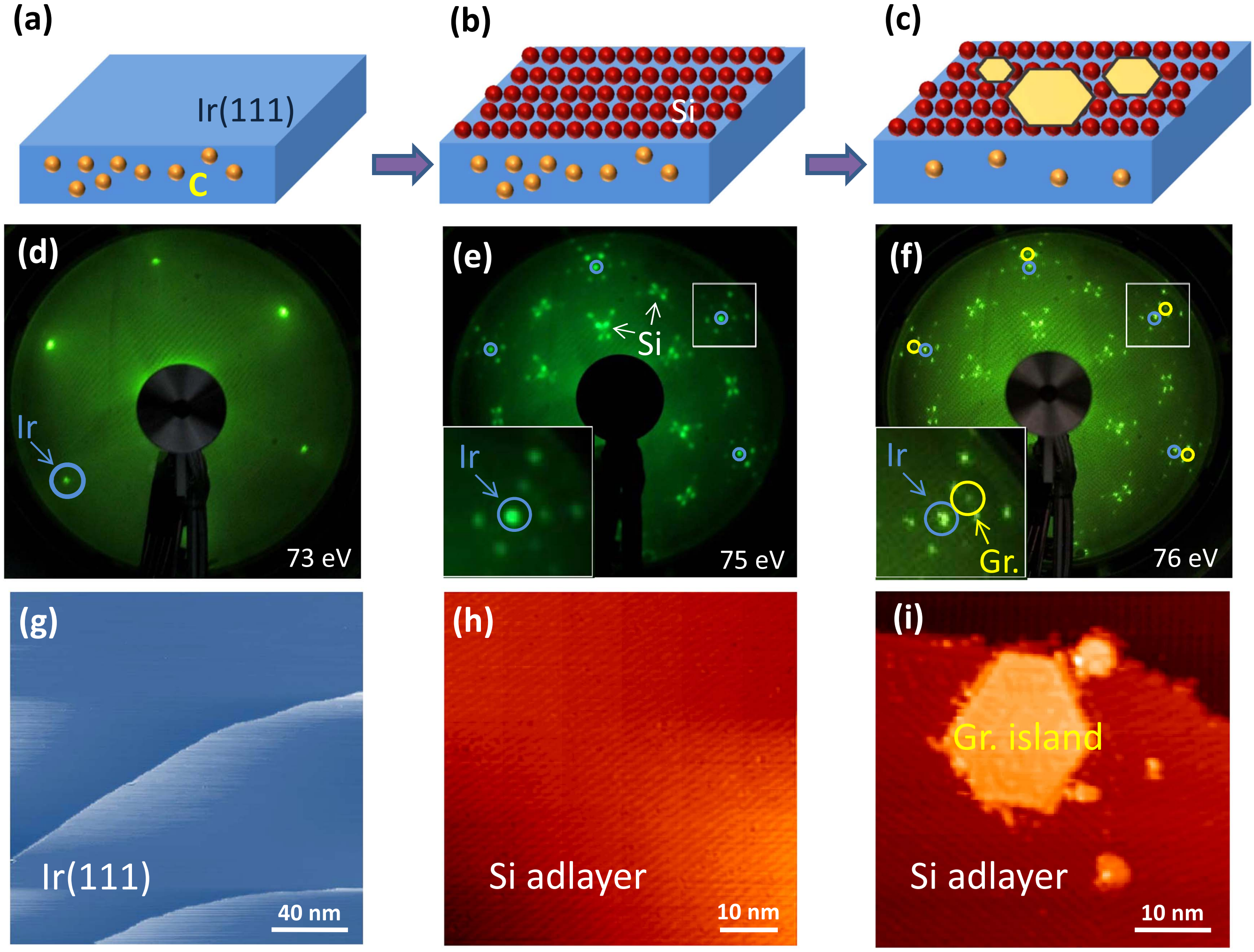

Figure 1. (a)–(c) Schematic of the fabrication process of two-dimensional graphene–silicon heterostructure. (d)–(i) LEED patterns and corresponding STM images of each procedure of fabricating the graphene–silicon heterostructure. (d) Before silicon deposition, the six bright spots indicated by the blue arrow are from the Ir(111) substrate with six-fold symmetry. (e) After silicon deposition and subsequent annealing, in addition to the six iridium diffraction spots, a group of new spots appears, denoted by the white arrow, indicating formation of a well-ordered structure consisting of silicon. (f) With further annealing, another six diffraction spots emerged, denoted by the yellow circle in the enlarged picture, which arise from the graphene lattice. (g) Large-scale STM image (−0.1 V, 0.11 nA) showing a clean Ir(111) surface. (h) STM image (−1.6 V, 0.16 nA) showing long-range ordered silicon superstructure. (i) STM image (−1.5 V, 0.1 nA) of graphene islands located on top of the silicon layer. (d)–(f) are obtained at 73 eV, 75 eV and 76 eV, respectively. The apparent heights are about 0.2 nm for the terraces of the Ir(111) substrate in (g) and about 0.1 nm for the graphene island in (i).

most importantly, the larger size of the graphene islands implies a trend of coalescence of small islands. We supposed that the small islands would eventually coalesce into larger islands with longer annealing time. As expected, after more annealing cycles, the number of small graphene islands decreased, as larger graphene islands formed on top of the silicon layer (see figure 2(d)).

To further examine the heterostructure, we selected typical graphene islands, aiming to investigate the arrangement of the two atomic layers. Figure 3(a) shows two hexagonal graphene islands on the surface of the silicon layer. Figure 3(b) is an atomic-resolution STM image of one graphene island. We know that single-layer graphene on Ir(111) substrate has an ordered moiré superstructure [24]. However, the graphene island here does not show an ordered moiré pattern, implying that bare iridium is not underneath the graphene island. This situation is similar to the intercalation between graphene and a metal substrate [25–28]. Therefore, the STM image (figure 3(b)) not only includes information about the graphene lattice, but also about the silicon superstructure beneath graphene. To understand this more clearly, we removed the silicon information part of the image from the fast Fourier transform (FFT) pattern by a high-pass treatment. Then, we got an image that nicely reveals the honeycomb lattice of the top atomic layer, demonstrating an intact and continuous layer, as shown in figure 3(c). Figure 3(d) shows the line profile along the black arrow in figure 3(c), revealing that the periodicity of the honeycomb lattice is about 0.25 nm. This distance is consistent with graphene lattice. Although the FFT treatment here only provides semi-quantitative information, the above analysis of the LEED pattern and STM images implies that the top atomic layer is graphene.

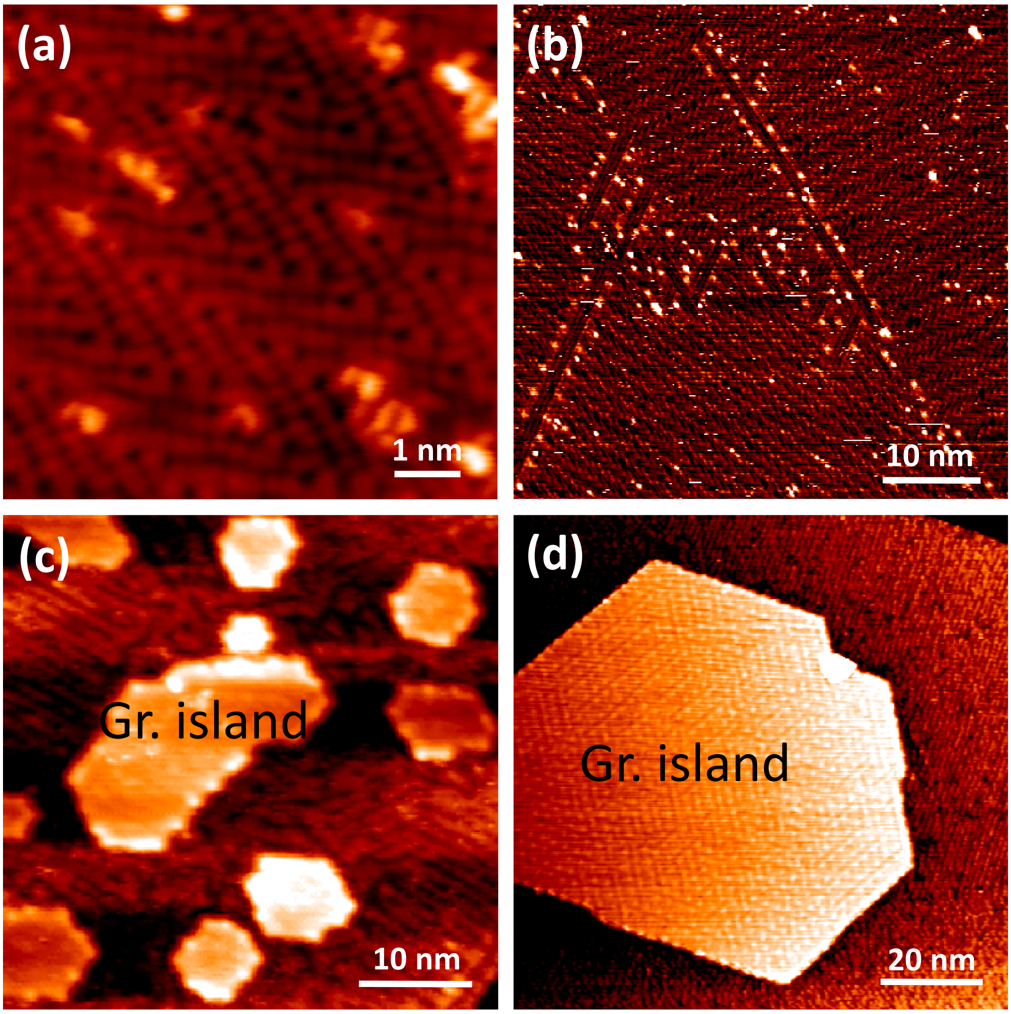

Figure 2. High-resolution STM images recording the evolution of the graphene islands. Small scale (−0.13 V, 0.31 nA) (a) and large scale (−1.67 V, 0.22 nA) (b) STM images showing that carbon atoms and clusters appear on the silicon layer after the first annealing cycle. (b) The carbon clusters arranged themselves regularly on the silicon layer. (c) Small graphene islands emerge after two more annealing cycles (−1.78 V, 0.05 nA). (d) After more annealing cycles, small graphene islands eventually coalesce into large graphene islands (−1.85 V, 0.03 nA).

In order to verify our understanding of the graphene–silicon heterostructure on Ir(111) from the macroscopic view, we employed Raman spectroscopy to characterize its physical properties. The sample was prepared by cycles of annealing after silicon deposition to obtain large graphene islands. As we expected, the two prominent Raman features of graphene, the G peak and 2D peak, emerge in the curve (figure 4), giving further assurance that a 2D graphene–silicon heterostructure had been successfully fabricated on the Ir(111) surface. Interestingly, graphene–silicon heterostructures can be fabricated by different methods. For example, graphene–silicon lateral and vertical heterostructures have been fabricated by a method of sequential deposition of carbon and silicon onto Ag(111) [29]. In our previous research, silicon was inserted into the interface of graphene and Ir(111) substrate by a method of intercalation [30, 31]. The technique presented here differs from previously reported methods. In the present work, we introduce a new technique of fabricating vertical graphene–silicon layered heterostructure by pumping carbon atoms located underneath a silicon layer. The thermal treatments of the sample drive the carbon atoms to penetrate to the top of the silicon and eventually coalesce into graphene islands there.

Conclusion

In summary, we report a new, easy, *in situ* technique for fabricating graphene–based heterostructures. The process was recorded by LEED and STM. Depositing silicon atoms onto an Ir(111) surface and subsequent annealing give rise to a silicon superstructure. With lengthening annealing time, carbon atoms stored in the bulk iridium penetrate to the top of the silicon layer and eventually coalesce into graphene islands there. Atomically resolved STM imagery, high-pass FFT treatment and Raman spectroscopy reveal that the topmost graphene layer is intact and continuous, and that beneath it is the silicon layer. The integration of graphene with a silicon layer combines two important electronic materials, offering the potential to discover new physical phenomena.

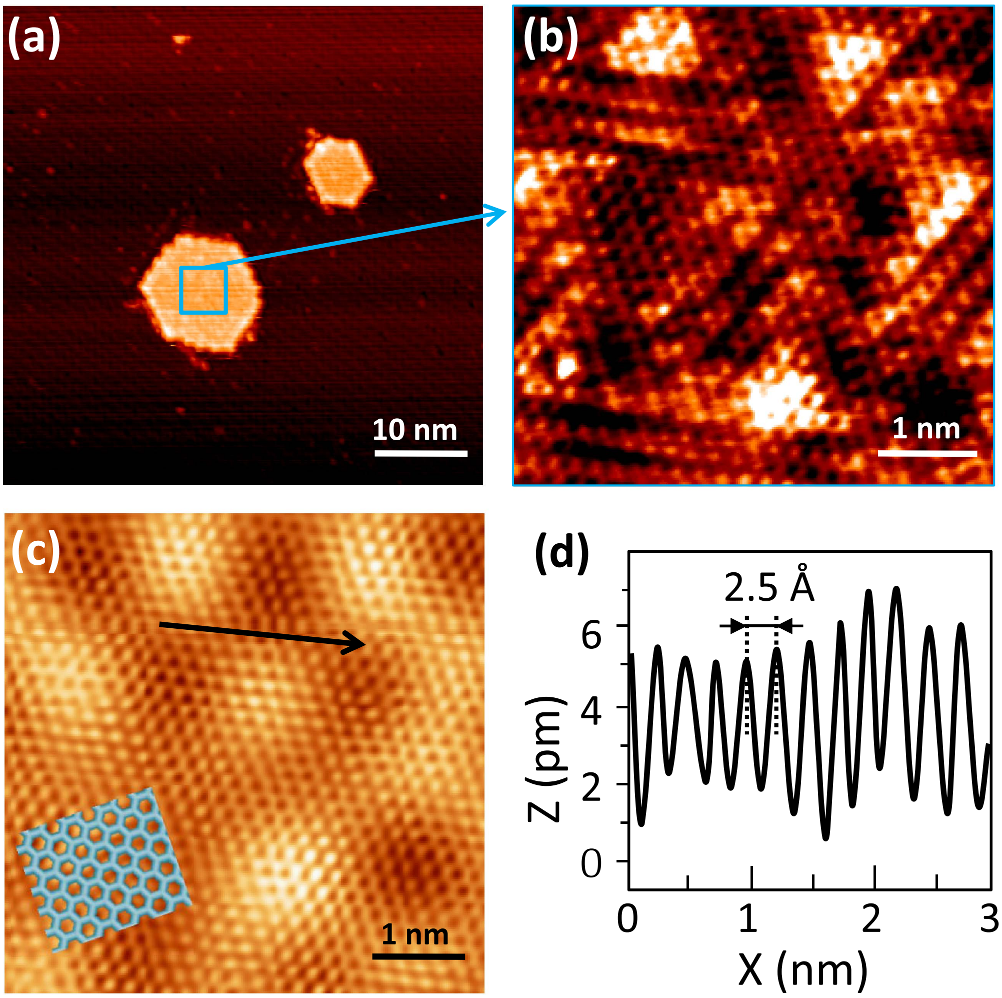

Figure 3. (a) STM image showing two typical hexagonal graphene islands on top of the silicon layer. (−1.71 V, 0.07 nA). (b) Atomically resolved STM image (−1.0 V, 0.1 nA) of graphene islands with silicon layer beneath. (c) Omitting the silicon information of (b) from the FFT pattern by a high-pass treatment, this image shows the intact honeycomb lattice. (d) Line profile along the black arrow in (c), revealing the periodicity of the honeycomb lattice (around 0.25 nm).

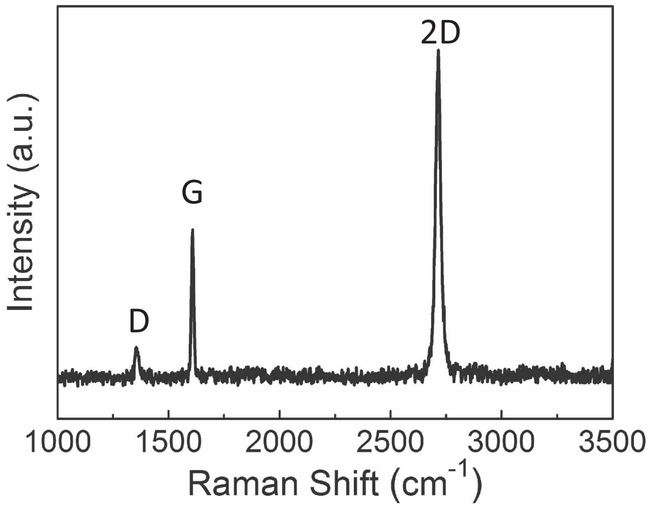

Figure 4. Raman spectrum at 532 nm for two-dimensional graphene-silicon heterostructure fabricated on Ir(111).

Acknowledgments

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