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Thick Layered Semiconductor Devices with Water Top-Gates: High On−Off Ratio Field-Effect Transistors and Aqueous Sensors

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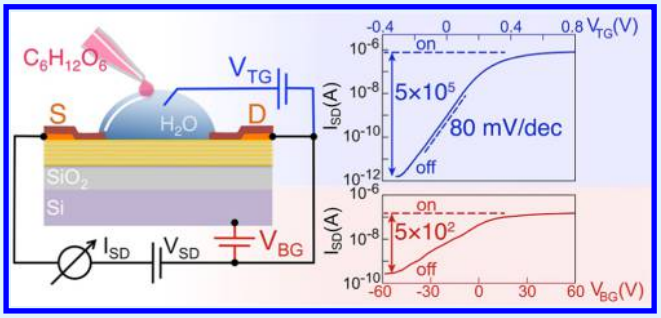
Supporting Information

ABSTRACT: Layered semiconductors show promise as channel materials for field-effect transistors (FETs). Usually, such devices incorporate solid back or top gate dielectrics. Here, we explore deionized (DI) water as a solution top-gate for field-effect switching of layered semiconductors including SnS_2, MoS_2, and black phosphorus. The DI water gate is easily fabricated, can sustain rapid bias changes, and its efficient coupling to layered materials provides high on−off current ratios, near-ideal subthreshold swing, and enhanced short-channel behavior even for FETs with thick, bulk-like channels, where such control is difficult to realize with conventional back gating. Screening by the high-k solution gate eliminates hysteresis due to surface and interface trap states and substantially enhances the field-effect mobility. The onset of water electrolysis sets the ultimate limit to DI water gating at large negative gate bias. Measurements in this regime show promise for aqueous sensing, demonstrated here by the amperometric detection of glucose in aqueous solution. DI water gating of layered semiconductors can be harnessed in research on novel materials and devices, and it may with further development find broad applications in microelectronics and sensing.



KEYWORDS: *field-effect transistor, layered semiconductors, tin disulfide, molybdenum disulfide, black phosphorus*

INTRODUCTION

Field-effect transistors (FETs), especially those made of silicon, play a central role in microelectronics.[1,2] Layered crystals, such as graphite, MoS_2, SnS_2, WS_2, and others whose electronic structure has long been known,[3−10] have only recently been considered as channel materials for FET devices.[11−14] One important reason is that although several layered semiconductors have sizable band gaps, carrier transport in thick, bulk-like crystals could not be modulated effectively by electrical fields due to screening and the resulting limited penetration of the gate electric field. The successful isolation of single-layer graphene opened new possibilities for field-effect devices by demonstrating that the carrier density in atomically thin devices can be tuned by moderate applied electric fields, even in semimetals.[15] Graphene FETs have shown very high carrier mobilities of up to 10^6 $cm^2/(V\ s)$, but the vanishing band gap limits their application in digital logic because graphene transistors cannot be turned off, i.e., show large off-state currents.[16] This limitation of graphene has led to efforts to exfoliate layered semiconductors, for example, transition-metal dichalcogenides such as MoS_2, to single-layer thickness for field-effect devices and the exploration of the fundamental properties of such monolayer semiconductors.[11,13,17,18] The on−off ratio in MoS_2 FETs, for example, reaches up to 10^8 at room temperature[11] and other two-dimensional (2D) semiconductors (WS_2, WSe_2, SnS_2, etc.) showed similar values, as well as a host of other fascinating properties.[19−26]

Previous studies of layered semiconductor FETs have mainly focused on single- and few-layer devices, and most reports to date involve channel thicknesses below 10 layers;[11,12] but in recent years, there have been a few reports on multilayer devices.[27−30] The interest in the ultrathin limit is in part driven by emerging properties due to the extreme carrier confinement in 2D crystals, but also reflects shortcomings of conventional gating strategies in controlling the conductance of thicker device channels. Back gating via a thick SiO_2 dielectric, the prevalent way of modulating electronic transport in studies of novel 2D and layered materials, offers relatively poor gate coupling and field penetration into layered crystals and hence cannot achieve high on−off current ratios in devices with thicker, bulk-like channels.[28] In addition, the back gate can affect the contact region and introduce unwanted features in the transistor characteristics, such as two conductance

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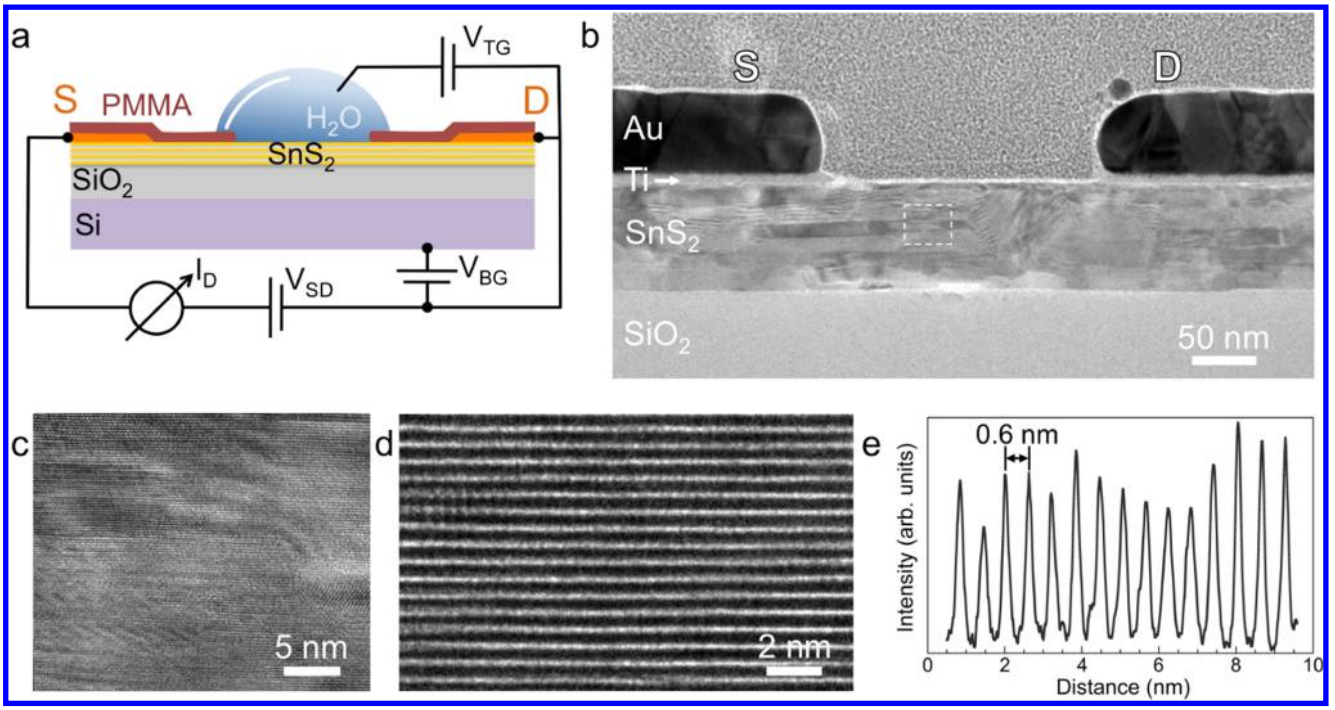

Figure 1. Schematic and cross-sectional TEM of a field-effect transistor (FET) with multilayer SnS_2 channel. (a) Schematic geometry of layered metal chalcogenide semiconductor based devices (e.g., with SnS_2 channel). S: source electrode; D: drain; V_{BG}: back-gate voltage, applied via the SiO_2/Si substrate; V_{TG}: top-gate voltage, applied via a deionized water solution gate, insulated by PMMA from the source−drain contacts. (b) TEM image of a FET device with 80 nm thick SnS_2 channel (~210 nm channel length) and Au/Ti contacts, supported on SiO_2/Si. (c) High-magnification view of the region of the SnS_2 channel marked in (b). (d) High-resolution TEM image, showing the SnS_2 layering. (e) Line profile showing a layer spacing of ~0.6 nm in the SnS_2 FET channel.

minima.[31] Side gates have been considered as an alternative, but they are typically difficult to fabricate and still offer limited control.[32] Top gates can achieve higher electric fields, but are also more difficult to fabricate and still provide limited control over the conductance of thick FETs. Ionic liquids[33,34] can be used to achieve very large electric fields in 2D and layered materials,[35] sufficient, for example, to induce superconductivity in MoS_2,[36,37] and lend themselves well for measurements in vacuum and at cryogenic temperatures. But ionic liquid gates face practical limitations. Slow charge transfer processes, for instance, require low bias scan rates to maintain equilibrium at the gate−channel interface. This calls for the development of alternative gating methodologies to study charge transport in layered materials and to harness the inherent advantages of FETs with thicker channels[27,38−40] compared to ultrathin single- or few-layer devices: higher current carrying capacity; lower Schottky barriers and hence reduced contact resistance at the layered semiconductor−metal junction;[41,42] and relative insensitivity to thickness fluctuations of the active layer, which facilitates a robust, high-yield device fabrication over large areas.

Here, we explore the use of a deionized (DI) water top gate[13,43,44] for field-effect tuning of the conductance of thick layered semiconductor FETs. This approach offers an alternative route toward efficient layered field-effect devices: instead of reducing the channel thickness to the ultimate 2D limit, the conductance of a thicker channel is switched between on and off states by a gate that supports very large electric fields at the channel surface. We find that the field penetrates sufficiently deep into the bulk that high on−off current ratios (up to 10^7) can be obtained for device channels up to several hundred layers thick. In addition, the efficient gating implies that short-channel effects can be largely suppressed even for thicker channels. Because liquid gate drops are simply dispensed onto the semiconductor surface and contacted by a suitable electrode, the fabrication challenges of the solid top-gate dielectrics are avoided. Gating via the double layer at the water−semiconductor interface supports much higher voltage sweep rates than ionic liquids. Finally, the use of an aqueous solution for gating provides facile access to water-based sensing, which we demonstrate here by detecting glucose with high sensitivity down to concentrations below 1 mM. Although we focus mainly on FETs with layered tin disulfide (SnS_2, a n-type semiconductor with ~2.3 eV band gap)[13] channels to illustrate the characteristics of DI water top gates, the approach is generally applicable to a broader class of layered semiconductors with inert as well as more reactive surfaces, as demonstrated for devices with thick MoS_2 and black phosphorus channels.

RESULTS AND DISCUSSION

Figure 1 illustrates the layout of the FET devices used here. The active channel consists of a layered semiconductor such as SnS_2, here prepared by exfoliation from high-quality bulk crystals to a typical thickness of 50−60 nm (~80−100 layers) and supported on a 300 nm SiO_2/Si substrate. The contacts (Ti/Au, 5/50 nm, see Experimental Methods for details) are covered by a thin polymer layer (poly(methyl methacrylate), PMMA type 950 A5, applied by spin coating at 3000 rpm) to electrically isolate them from the gate, which consists of a DI-water drop applied by a pipette. The device can be gated alternatively by a top-gate voltage (V_{TG}) applied to an electrode in contact with the water drop, or by back gating (V_{BG}) via the SiO_2 support (Figure 1a). Figures 1b−d show

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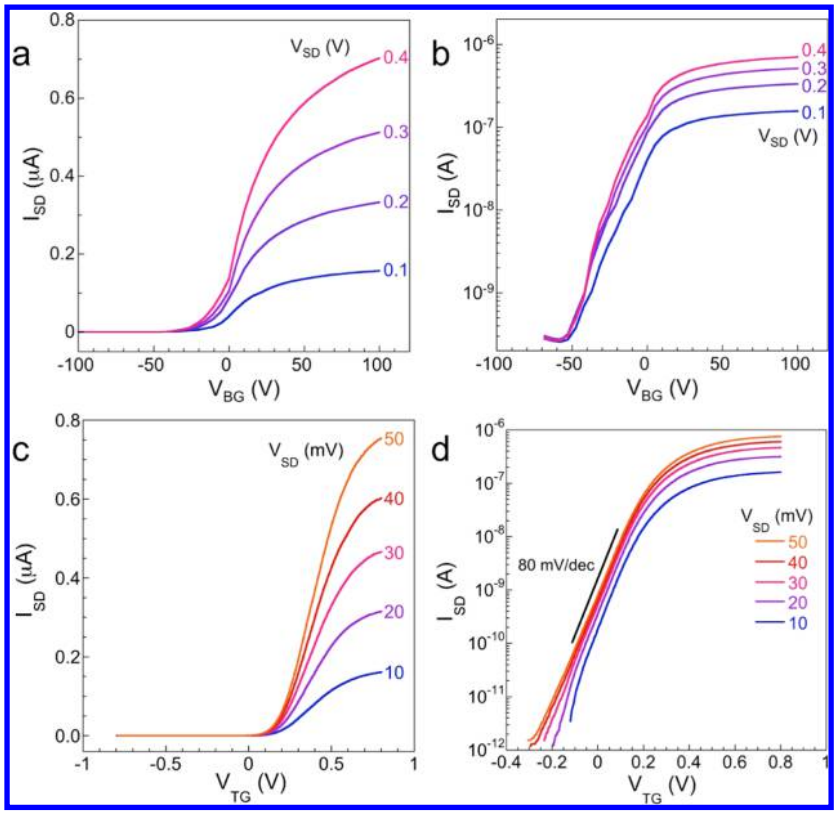

Figure 2. Device characteristics of a thick (~70 nm) SnS_2 FET device. (a) Linear and (b) logarithmic plots of the $I_{SD}-V_{BG}$ transfer characteristics of the back-gated FET for source–drain bias V_{SD} ranging from 0.1 to 0.4 V. The on–off ratio is about 3×10^3. (c) Linear and (d) logarithmic plots of the $I_{SD}-V_{TG}$ transfer characteristics of the solution top-gated FET for source–drain bias V_{SD} ranging from 10 to 50 mV. The on–off ratio now exceeds 8×10^5 and the subthreshold swing is ~80 mV/dec. Note also the substantially higher on-state current with DI water top gating, e.g., 0.8 μA at V_{SD} = 50 mV compared to 0.16 μA at V_{SD} = 100 mV with back gating. Gate voltages were swept from negative to positive in the measurements shown here and below.

cross-sectional transmission electron microscopy (TEM) images of one of the fabricated devices (without the PMMA insulator layer). The active region, ~82 nm thick, is mostly homogeneous but shows a number of stacking faults and embedded smaller grains. In higher-magnification TEM images, the layered structure is clearly visible (Figure 1c,d) with a periodicity of ~0.6 nm (Figure 1e), consistent with the layer spacing of SnS_2.[13]

A direct comparison of the transfer characteristics of devices with back and solution top gating demonstrates the striking effects due to the high electric fields at the water/layered metal dichalcogenide interface. The electric field applied via the SiO_2 back gate fails to bring the thick (~70 nm) SnS_2 channel efficiently into its off state, even for large applied voltages (Figure 2a). This is evidenced by an on–off current ratio of ~3×10^3 over a back gate voltage range $-100 \le V_{BG} \le 100$ V, as well as a relatively large "off-state" source–drain currents, $I_{SD} \sim$ 0.2 nA (Figure 2b). Negative gate bias voltages greater than −50 V are needed to bring the device into this off state (Figure 2b). The same device controlled by DI water top gate shows substantially improved transconductance characteristics. I_{SD} is now efficiently modulated via small changes in gate bias, $|V_{TG}| < 1$ V (Figure 2c) and the channel is efficiently turned off, as demonstrated by on–off ratios exceeding 10^5 (Figure 2d). These values are sufficient for practical, low-voltage operation of layered metal chalcogenide-based field-effect devices. Similar behavior is observed for other materials. Figure 3 shows examples of device characteristics of FETs with thick MoS_2 and black phosphorus channels. As for SnS_2, a comparison of back gating via the 300 nm SiO_2/Si support with top gating by DI water shows significantly enhanced on–off ratios with the solution gate, even for channels with thickness of several tens of nanometers. The demonstration of this effect for three materials, SnS_2, MoS_2, and black phosphorus supports the generality of our findings independent of the specific layered crystal used for the active channel of the FET.

Top gating by DI water not only enhances the field penetration of thick device channels, allowing them to be turned off completely, but it also improves the current hysteresis during gate bias sweeps and results in a substantially higher carrier mobility. These improvements are illustrated in Figure 4 for SnS_2 field-effect transistors. The FETs fabricated from layered materials often show significant hysteresis, assigned primarily to charge trapping by surface and interfacial trap states.[45,46] As can be seen in Figure 4a, the transfer characteristic of back-gated SnS_2 devices indeed shows this hysteresis upon reversal of the gate bias sweep direction. For this device, the current ratio between positive and negative gate bias is 67 over a gate voltage range from −35 to +40 V. When controlled by DI water top gate, the same device shows almost no detectable hysteresis upon reversal of the gate voltage sweep direction (Figure 4b), which implies that charge traps are no longer active after the water drop is applied. This behavior is consistent with the absence of surface adsorbates in the solution environment and an effective screening of interface states[11,47] by the high-k dielectric ($\varepsilon_{rel}(H_2O)$ ~

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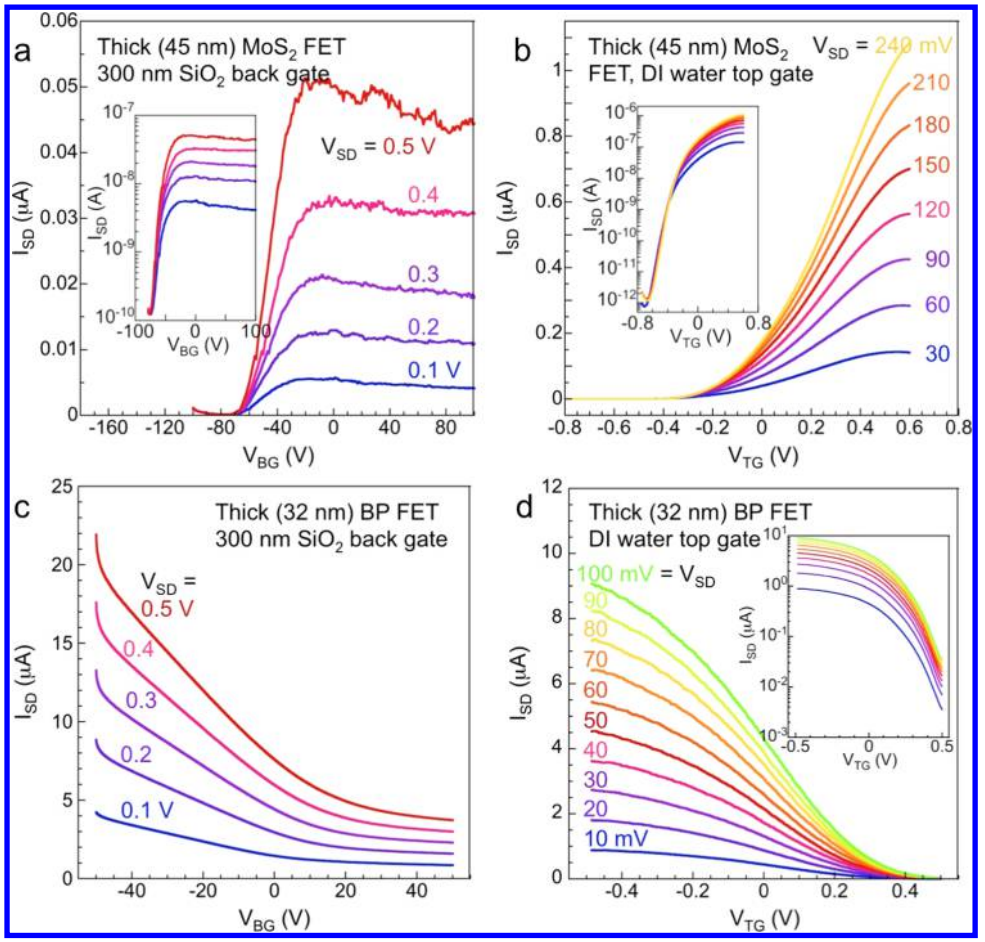

Figure 3. Characteristics of thick MoS_2 and black phosphorus FETs. (a) $I_{SD}-V_{BG}$ transfer characteristics of a back-gated MoS_2 FET with 45 nm channel thickness for source–drain bias V_{SD} ranging from 0.1 to 0.5 V. Back-gate voltages greater than −60 V are required to bring the device into the off state. The logarithmic plot shown in the inset displays an on–off ratio below 10^3. (b) Transfer characteristic of the same MoS_2 FET controlled by a DI water top gate for applied source–drain bias between 30 and 240 mV. Note the significantly higher on-state current of the water-gated device, e.g., >0.9 μA compared to 0.01 μA for back gating at $V_{SD} \sim 200$ mV. The logarithmic plot given in the inset shows an on–off ratio of $\sim 10^6$ of the top-gated device. (c) $I_{SD}-V_{BG}$ transfer characteristics of a back-gated black phosphorus FET with 32 nm channel thickness for source–drain bias V_{SD} ranging from 0.1 to 0.5 V. (d) Transfer characteristic of the same black phosphorus FET controlled by a DI water top gate (V_{SD} between 10 and 100 mV; inset: logarithmic representation) showing a reduced off-state current of the solution-gated device.

80).[48] Qualitatively similar results have also been reported for thin MoS_2 FETs employing HfO_2 or Al_2O_3 top gates.[49−51] Again, solution top gating provides significantly enhanced transfer characteristics compared to back gating, with a high on–off ratio of $\sim 5 \times 10^5$ and a near-ideal subthreshold swing of 80 mV/dec (Figure 4b). To compare the field-effect electron mobility for the two gate types, the mobility has been calculated from the transconductance characteristics via $\mu = \frac{dI_{SD}}{dV_G} \cdot \frac{L}{WCV_{SD}}$. The particular transistor considered in Figure 4 has an aspect ratio $L/W = 3$, and the gate capacitance is either $C(SiO_2) = 11.6$ nF/cm^2 (back gate[52]) or $C(H_2O) = 137$ nF/cm^2 (top gate), the double-layer capacitance of the DI water gate in contact with a SnS_2 FET channel determined previously.[13] The field-effect mobility increases from 50 cm^2/(V s) (back gated) to 180 cm^2/(V s) (top gated). This increase due to screening of scattering centers by the liquid dielectric is less pronounced than in the case of thinner few-layer or monolayer SnS_2 FETs because surface and interface scattering play a relatively smaller role in the devices with thick channel considered here. Measurements of the on–off ratio on devices with different channel thickness (Figure 4c) demonstrate that the overall gains due to liquid gating are nearly independent of the thickness of the active layer, so that on–off current ratios greater than 10^5 can be maintained for bulk-like channels up to at least 200 nm in thickness. The systematic dependence on the channel thickness seen in Figure 4c clearly demonstrates that the enhancements in the on–off ratio achieved by replacing back gating with DI water top gating are substantially larger than possible fluctuations from device to device. The ultimate limit of double-layer top gating has been probed in ionic liquid-gated transistors fabricated from bulk SnS_2 single crystals.[53] Similar to the DI water electrolyte gating reported here, ionic liquids electrostatically control charge in the active channel through ions in the interfacial double layer. In this way, using a *N*,*N*-diethyl-*N*-methyl-*N*-(2-methoxyethyl)ammonium bis-(trifluoromethanesulfonyl)imide ionic liquid, even FETs with a ~300 μm thick SnS_2 could be controlled with an on–off ratio of ~100.[53]

Layered semiconductors may offer superior scaling and improved short-channel characteristics compared with silicon FETs. We fabricated FETs with channel length ranging from 2 μm to 200 nm to compare the scaling of SnS_2 FETs with SiO_2 back gate and DI water top gate (Figure 5a). Devices with thin

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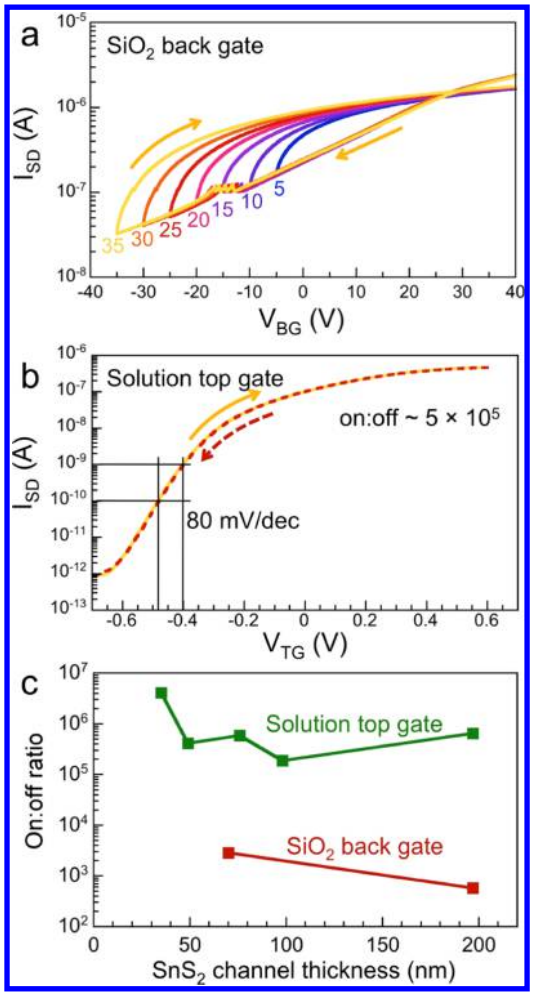

Figure 4. Hysteresis and dependence of on−off current ratio on channel thickness for SnS_2 FETs. (a) Transfer characteristics of a back-gated FET, scanned from +40 V to negative gate voltages between −5 and −35 V. Note the significant hysteresis as the V_{BG} sweep direction is reversed, and the modest change in current (factor ∼ 67) between positive and negative gate bias. (b) Transfer characteristic of the same device with DI water top gating (same gate voltage sweep rate as in (a)). Note the absence of hysteresis, large on−off current ratio (∼5 × 10^5), and near-ideal subthreshold swing (80 mV/dec). (c) Comparison of the on−off current ratios as a function of channel thickness for devices controlled by back gating and solution top gating.

(∼8 nm) and long channel show consistently high on−off ratios (>10^6), both controlled by back gating and solution top gating. However, for channel length below ∼800 nm, the on−off ratio of back-gated devices drops below 10^5, whereas that of the top-gated devices remains high (Figure 5b). Similarly, the on−off ratio of FETs with thick (55 nm) SnS_2 channel controlled by DI water top gates remains high (∼10^6) over the entire range of channel lengths considered here (Figure 5b). This suggests that the very high electric fields achievable at the solid−liquid interface can effectively prevent possible leakage due to a finite source−drain bias at short channel lengths, so that the off current remains low at least down to the shortest channels considered here (200 nm). This beneficial effect applies to both ultrathin devices, which have been considered extensively before,[42,54] and thicker, bulk-like layered semiconductor devices that are the focus of the present work. The observed trends can be understood within a framework developed for scaling in silicon, which invokes the characteristic length $\lambda = \sqrt{(\varepsilon_s/\varepsilon_{ox})\cdot\tau_s\tau_{ox}}$, determined by the permittivities and thicknesses of semiconductor (ε_s, τ_s) and gate dielectric (ε_{ox}, τ_{ox}).[55] Within this picture, FETs with ultrathin channel have smaller λ, i.e., can be scaled to smaller dimensions. On the other hand, the thick devices considered here accentuate differences in short-channel effects between back gating and solution top gating by showing consistently high on−off ratio with solution gating. The superior performance of the solution gate results from a combination of high permittivity ($\varepsilon \sim 80$) and small thickness (∼5−10 nm) of the double-layer gate. Our results therefore suggest that the combination of a solution top gate with a relatively inert layered semiconductor active region, which forms a stable interface with aqueous solutions, can allow harnessing the advantages of thicker FET channels while still permitting scaling to short channel lengths.

The thick layered (SnS_2, MoS_2, and black phosphorus) field-effect transistors discussed here are depletion-mode devices. For V_G = 0, the channel has finite conductance. For the n-channel materials SnS_2 and MoS_2, application of a negative gate bias causes the expansion of a depletion region, which decreases and ultimately turns off the charge transport through the channel (the analogous effect occurs at positive bias in p-channel black phosphorus FETs), whereas positive gate voltages increase the carrier density. Both carrier depletion and accumulation depend on the gate-induced electric field across the entire channel. In the case of back gating, the layers close to the SiO_2 interface are optimally controlled by the gate and the electrostatic control is weakened gradually in the semiconductor layers further away from the SiO_2 interface due to charge screening. Besides screening in the bulk, interfacial traps can strongly affect the electrostatic gating by further reducing the penetration of the electric field into layers away from the interface to the gate dielectric. Within this picture, three main factors determine the gate control, described here via the on−off ratio: (i) the magnitude of the electric field at the gate−channel interface; (ii) the Debye length in the semiconductor; and (iii) the density of interfacial traps. The Debye length can be assumed to be an intrinsic materials property unless there are additional effects, such as intercalation (see below). For DI water top-gated devices, achieving similar magnitude of the field at the interface requires substantially lower applied gate voltages than for back gating via 300 nm SiO_2. However, this does not explain the large off-state and reduced on-state currents of back-gated layered FETs. Hence, the most likely explanation for the difference in on−off ratio between back gating and DI water top gating is the additional screening by interfacial traps. As shown in Figure 4, hysteresis due to such trap states is invariably observed in the back-gated SnS_2 FETs, but is no longer detected in the same devices operated with DI water top gate. Along with the elimination of the hysteresis, the on−off ratio increases substantially. For thick back-gated SnS_2 devices, the relevant traps are located at the SiO_2/SnS_2 interface, whereas surface traps would affect ultrathin (mono- or few-layer) devices but would be less important for the FETs with thick multilayer channels studied here. Conversely, for solution top-gated devices, surface traps affect the gate control more strongly than trap states at the substrate interface. The absence of hysteresis in Figure 4b suggests that the effects of such surface trap states are essentially eliminated in devices

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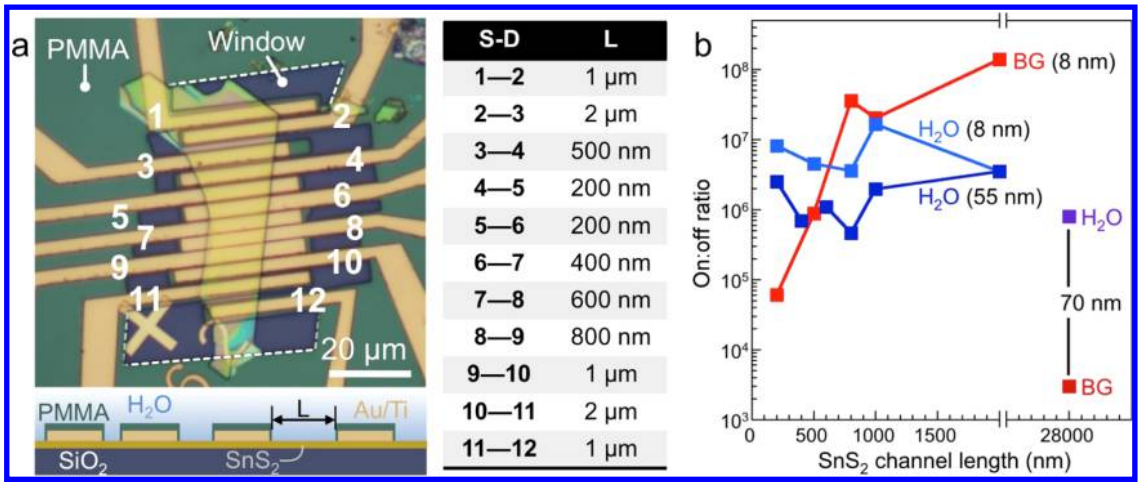

Figure 5. Short-channel effects as reflected in the on−off ratio. (a) Optical micrograph of the device layout of SnS_2 FETs with different channel lengths ranging from 200 nm to 2 μm, along with a schematic of the PMMA contact encapsulation (bottom) and a table of the channel length (L) for different contact geometries (right). The channel length L corresponds to the portion of the channel contacted by water, i.e., the size of the PMMA window. (b) Channel length scaling for SnS_2 devices with thin (8 nm, ∼13 layers) channel (BG: back-gated; H_2O: DI water top-gated), in comparison with SnS_2 devices with thick (55 nm) channel (DI water top-gated). Symbols on the right represent the on−off ratio of the long-channel FET (L = 28 μm) whose transfer curves are shown in Figure 2.

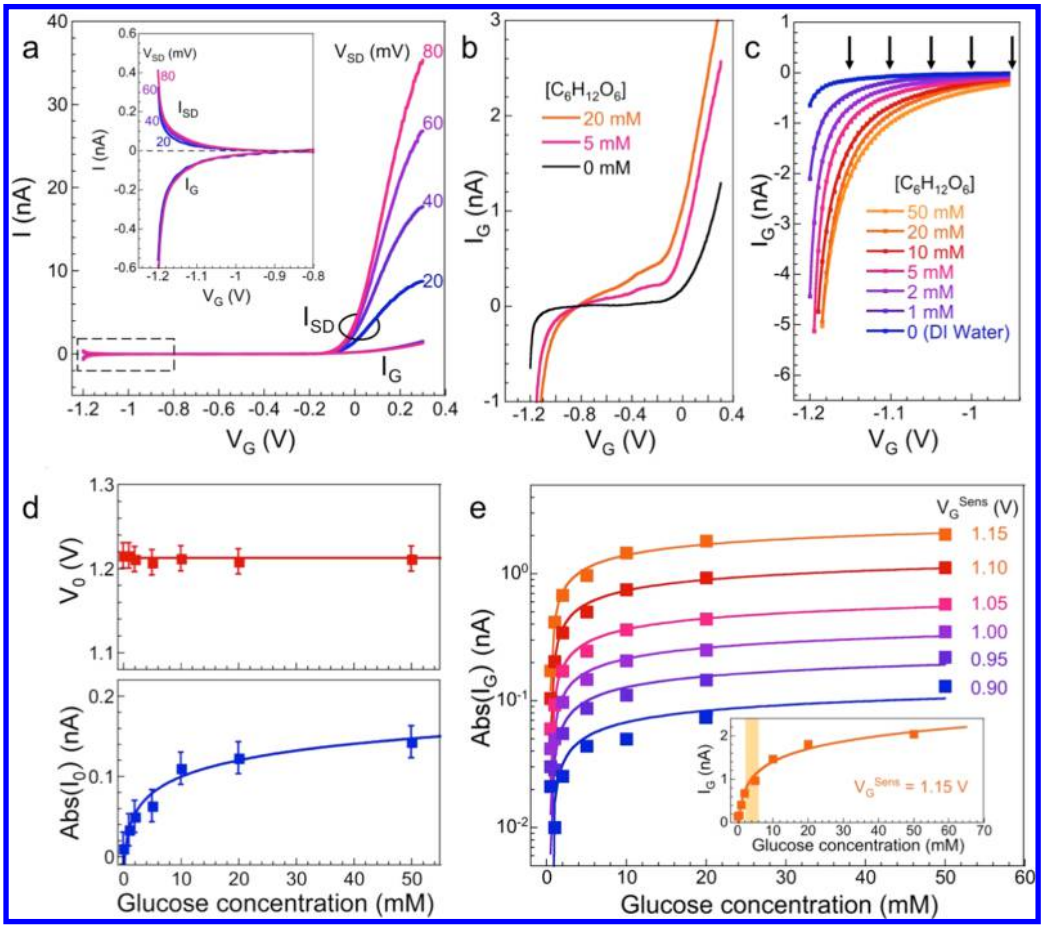

Figure 6. Gate current and its use for aqueous sensing. (a) Source−drain current (I_{SD}) and gate current (I_G) of a FET with thick SnS_2 channel as a function of gate bias, applied to the DI water top gate. The zone of increasing I_G at large negative gate voltage, marked by a dashed rectangle, is shown at higher magnification in the inset. (b) Response of the gate current to increasing concentrations of glucose in the DI water gate. (c) Systematic change in gate current with increasing concentration of glucose in the DI water gate at a large negative gate voltage. Lines are fits of $I_0/(V_G - V_0)$ to the data. (d) Summary of the fit parameters derived from (b), showing a constant asymptote voltage V_0 but a logarithmically increasing current amplitude Abs(I_0) (solid blue line: log fit) with increasing glucose concentration. (e) Glucose sensing via the gate current, Abs(I_G), at different fixed gate voltages (labeled; also indicated by arrows in (c)). Lines are logarithmic fits to the data. The inset indicates a detection limit below 1.0 mM glucose concentration.

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controlled by a DI water top gate. Previous studies have implicated adsorbed water molecules as both surface and interfacial traps in monolayer MoS_2 FETs.[45,46] Covering the channel surface with DI water appears to suppress the effects of adsorbates on the free surface and hence allows better gate control due to reduced screening by trap states at the gate−channel interface of the DI water-gated devices. A direct comparison between back gating and DI water top gating for the same devices (e.g., in Figure 2 for thick SnS_2 FETs) suggests that the elimination of screening by surface traps causes both an increase in the on-state current and a suppression of the off-state current in the solution top, which jointly give rise to enhanced on−off ratios.

In addition to the above considerations, which would apply independent of the channel material (e.g., also for a wide range of other channel materials, such as ordinary three-dimensional inorganic crystals or organic semiconductors),[56] there are two possible additional mechanisms—both related to the edges of the active channel region—that may play a role in enhancing the on−off ratio of thick layered field-effect transistors gated by DI water. A first possible mechanism involves a predominant transport along the edges of layered materials. If conduction along the edge is important, once ions in the solution gate move to the edge sites, they will be able to control the current in the edge conduction channels, independent of the channel thickness. A second possible mechanism involves intercalation between the individual sheets in layered materials. This phenomenon was reported, for example, for layered FeSe superconductors in contact with ionic liquids (with residual water molecules), for which protonation between the layers driven by applied bias was observed to increase the superconducting transition temperature.[57] In our DI water-gated devices, the concentrations of H^+ and OH^- ions are substantially higher than those in ionic liquids and hence, if intercalation takes place, the ions can intercalate readily from the edges into SnS_2, MoS_2, or black phosphorus flakes. For example, when a negative bias is applied to the DI water gate, H^+ ions move to the gate electrode, whereas OH^- ions move into the layered semiconductor, e.g., SnS_2. The intercalated negative ions can decrease the concentration of majority carriers (electrons) in the SnS_2 crystal, decreasing the off current. Conversely, for positive gate bias H^+ ions driven to intercalate could increase the carrier density. In this case, the gating should again be largely independent of the channel thickness, as seen in Figure 4c, as long as the edges are open and accessible to the ions in the solution. Although more experiments are needed to fully identify the mechanism underlying the efficient gating of thick layered FETs by DI water, preliminary results highlight the importance of contact between the solution gate and the channel edges. The supporting Figure S1 compares two different devices gated by DI water: one in which the entire channel (including the edges) is covered by the solution gate (Figure S1a) and the other in which the edges have been covered by polymer (PMMA, Figure S1b). We find that both devices show some degree of gate control, but whereas a small negative gate voltage (−0.1 V) is sufficient to turn off the current flow in the device with open edges, the device with insulated edges still shows significant conductance at a higher negative gate voltage (−0.5 V). These data lend further support to the notion that access of the gate solution to the channel edges may be important for field-effect devices with thick layered crystal channels.

We now explore in more detail the properties of the DI water top gate itself, in particular the possibility of the current flow through the gate electrode (i.e., gate leakage). The gate current I_G in top-gated SnS_2 devices was measured simultaneously with I_{SD} as the top gate bias V_G was swept for different applied source−drain voltages, V_{SD}. Representative results of these measurements are shown in Figure 6a. The FET transconductance characteristics at different V_{SD} reflect the same behavior observed for other devices (e.g., Figure 1), i.e., efficient control of I_{SD} by the solution gate. Although the device is clearly in its off state for gate bias between −0.2 and −1.0 V, the current starts to increase again for a larger negative V_G. The measurements shown in Figure 6a indicate that this behavior is not due to the ambipolar conduction that has been reported previously for some layered semiconductors, such as bulk and ultrathin WSe_2.[17,58] For example, the magnitude of I_{SD} is independent of the source−drain bias, in contrast with the expected behavior for ambipolar FETs. Simultaneous measurements of the gate current show the same onset of increased current for $V_G \sim -1.0$ V, mirroring the behavior observed in I_{SD}. Hence, we attribute the apparent rise in I_{SD} to a rapidly increasing current flow across the gate junction at large negative bias. Note that for positive V_G, there is consistently only a small amount of gate leakage, limited to ∼10% of I_{SD} for small V_{SD} (20 mV) and below 3% of I_{SD} for larger V_{SD} (80 mV).

The ultimate limit of DI water solution gating is set by electrochemical reactions involving the reduction or oxidation of the electrodes and of the solution itself at large gate bias. Large positive bias, for example, could drive the oxidation of the cathode (the SnS_2 channel) and the concomitant reduction of the anode (the gate contact), whereas opposite effects would occur at large negative bias. We explore the limit for the negative gate voltage range in more detail. Further analysis (see below) shows that the absolute value $\mathrm{Abs}(I_G)$ increases asymptotically to large values at an applied bias of (-1.21 ± 0.05) V, close to the standard potential for electrolysis of water (−1.23 V). The onset of electrolysis may therefore set an ultimate limit to the operating range of a DI water top gate, but our two-electrode setup limits the obtainable information. If confirmed by additional electrochemical experiments, our data suggest that the SnS_2 cathode (the FET channel) may act as an efficient electrocatalyst that facilitates water electrolysis with minimal overpotential. At the same time, the chemically inert nature of the sulfur-terminated surface of layered SnS_2 ensures that no (electro-) chemical reactions occur with the channel material. Highly reproducible characteristics of the miniature electrochemical cell in our DI water top-gated SnS_2 FETs (Figure 6a) raise the possibility that the gate current could be used for aqueous sensing. In the simplest case, it should be possible to detect the presence of ionic solutes, either via an increase in conductivity across the solution gate or through changes in the FET transfer characteristics (i.e., I_{SD}). Here, we demonstrate a less straightforward example of aqueous sensing, the measurement of the concentration of glucose—a nonionic solute—in water.

Figure 6b shows changes in the I_G-V_G characteristics with increasing glucose concentration $[C_6H_{12}O_6]$ in the DI water gate drop both for positive and negative bias. At positive voltages, the gate current increases with glucose concentration but shows no well-defined (e.g., linear) relationship (Figure 6b). Figure 6c shows an enlarged view of the data for a number of different glucose concentrations at negative gate voltages

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near the electrolysis threshold. A stepwise increase in $[C_6H_{12}O_6]$ causes well-defined changes in the I_G−V_G curves. To quantify these changes, the measured data were fitted by an empirical function $I_G = I_0/(V_G - V_0)$, which correctly represents the strongly increasing (i.e., essentially diverging) gate current at the electrolysis potential (V_0). The fit results are shown as lines in Figure 6c and summarized in Figure 6d. According to the analysis, the change in glucose concentration affects only the current amplitude (I_0) but not the asymptotic electrolysis potential (V_0), which remains constant for all values of $[C_6H_{12}O_6]$ probed here (0−50 mM). Abs(I_0) rises logarithmically with increasing glucose concentration (Figure 6d). This behavior, which may be due to the adsorption of glucose molecules and a resulting change in the double-layer capacitance, can form the basis for a simple amperometric scheme to measure the glucose concentration, which is detected via the gate current I_G at any fixed gate bias near the electrolysis threshold ($V_G \leq -0.9$ V). As shown in Figure 6e, any choice of V_G^{sense} in this range will give the same logarithmic dependence of I_G on $[C_6H_{12}O_6]$, with a detection limit below 1 mM and a high sensitivity in the concentration range corresponding to the physiological glucose levels in human blood (∼4−6.5 mM). The gate current is reversible, and after removing glucose followed by rinsing in DI water, the original characteristics with pure DI water gating are recovered. This suggests that the SnS_2 channel itself remains unaffected by the conditions used for glucose detection. We note that although our data show the ability to sense glucose via an electrical signal in SnS_2-based FETs, additional work is needed to identify the precise sensing mechanism for nonionic solutes, i.e., the origin of the change in gate current as a function of glucose concentration and to probe the specificity to a single solute in the presence of other species in an aqueous solution. It is also possible that other electrode materials could provide similar sensing characteristics for aqueous glucose solutions. To probe this possibility, we examined control samples with chemically reactive (Cu) and inert (Au) metal thin films as working electrodes. Measurements on Cu films (Figure S2) show clear signs of irreversible changes, and no systematic dependence of the current on the glucose concentration is found. In contrast, thin Au electrodes (Figure S3) show reproducible characteristics with concentration dependence similar to that of the SnS_2 device. These control measurements lend further support to SnS_2 as a versatile, chemically stable electrode material for aqueous sensing applications. The incorporation of additional enzymatic components, e.g., glucose oxidase used in conventional sensors,[59] may be required to achieve specific sensing. Beyond the static gate solutions used here, one can foresee the integration of SnS_2 devices in microfluidic platforms for real-time electrical sensing of aqueous solutes.

CONCLUSIONS

We have demonstrated solution gating by deionized water as a method to achieve field-effect control over the conductance of a wide range of layered semiconductors, including SnS_2, MoS_2, and black phosphorus. The efficient coupling and large electric field of the solution gate provides high on−off current ratios, a near-ideal subthreshold swing, and enhanced short-channel behavior even for bulk-like channels with a thickness of several 10 nm to well over 100 nm. Other advantages of the solution top gate include facile fabrication compared to conventional approaches involving solid dielectrics, and the capability of applying rapid changes in gate bias unlike ionic liquid gates that require slow bias ramps. Screening of the surface and interface trap states by the high-k solution gate eliminates the gate-bias hysteresis found for back-gated devices and substantially enhances the field-effect mobility. These favorable characteristics of DI water gating in FETs can readily be leveraged in materials and device research, and they may find applications in microelectronics if suitable encapsulation strategies for a liquid gate can be identified. The onset of water electrolysis and associated leakage currents sets the ultimate limit to DI water gating at large negative gate bias. Measurements in this regime show promise for aqueous sensing, explored here by the amperometric detection of glucose in static drops down to concentrations of ∼1 mM. By incorporating layered semiconductor FETs into microfluidic platforms, this approach could be expanded to allow a high-throughput sensing in aqueous solutions.

EXPERIMENTAL METHODS

Sample Preparation. Adhesive tape was used to exfoliate layered bulk crystals (SnS_2, MoS_2, black phosphorus). It was folded 2−3 times to make the bulk crystal thinner. The tape with SnS_2 (or other layered material) was then put onto the surface of a SiO_2/Si (300 nm) substrate cleaned by oxygen plasma. Before peeling off the adhesive tape, the substrate together with layered crystal/tape was put on a hot plate to anneal for 1−2 min at 100 °C to improve the contact area between the layered crystal and SiO_2 surface and obtain large flakes.[60]

Device Fabrication and Electrical Measurements. After the transfer of SnS_2 (or MoS_2, black phosphorus) flakes to SiO_2/Si substrates by mechanical exfoliation, optical microscopy was used to identify selected flakes with different thickness; the thickness was measured by atomic force microscopy. Photoresist was spin-coated onto the substrates (S1811, 3000 rpm, 1 min) and annealed on a hot plate at 110 °C for 2 min. Devices were patterned by UV photolithography (mask aligner Karl Suss, MA6). Ti/Au (5/50 nm) contact metallization was performed in a lift-off process by e-beam evaporation, followed by photoresist dissolution in acetone. The devices were annealed in ultrahigh vacuum (10^{-9} Torr) to enhance the contact resistance. Electrical measurements were performed on a four-probe station (Signatone). For DI water top-gated FETs, an additional PMMA layer (type 950 A5) was deposited on the devices (spin coating at 3000 rpm; thickness ∼400 nm), baked at 180 °C for 2 min, and patterned by electron-beam lithography to open windows for contact between the water drops and the device channel. After the application of the DI water gate drops, devices could be measured for up to 1 h before the drop evaporated, depending on relative humidity. Repeated I−V measurements on the same devices showed no signs of degradation during this period. (Dry) devices could furthermore be stored in air for extended time periods (months) without degradation. All electrical measurements were carried out at room temperature in air.

Transmission Electron Microscopy on Complete Devices. Fully functional FET devices were covered in platinum and prepared into electron transparent cross-section specimens by focused ion beam (FIB) milling using a FEI Helios dual beam FIB instrument, followed by transfer to TEM grids. The FIB sections included the device channel and the adjacent source and drain contacts. TEM imaging was performed in a FEI Tecnai Osiris ChemiSTEM microscope at 200 kV beam energy.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.8b05932.

DI water gating with open and protected channel edges (Figure S1); two-terminal measurements of glucose in

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DI water with metallic electrodes (Cu, Figure S2; Au, Figure S3) (PDF)

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