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Research Article

InSe/hBN/graphite heterostructure for high-performance 2D electronics and flexible electronics

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ABSTRACT

Two-dimensional (2D) materials as channel materials provide a promising alternative route for future electronics and flexible electronics, but the device performance is affected by the quality of interface between the 2D-material channel and the gate dielectric. Here we demonstrate an indium selenide (InSe)/hexagonal boron nitride (hBN)/graphite heterostructure as a 2D field-effect transistor (FET), with InSe as channel material, hBN as dielectric, and graphite as gate. The fabricated FETs feature high electron mobility up to 1,146 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at room temperature and on/off ratio up to 10^{10} due to the atomically flat gate dielectric. Integrated digital inverters based on InSe/hBN/graphite heterostructures are constructed by local gating modulation and an ultrahigh voltage gain up to 93.4 is obtained. Taking advantages of the mechanical flexibility of these materials, we integrated the heterostructured InSe FET on a flexible substrate, exhibiting little modification of device performance at a high strain level of up to 2%. Such high-performance heterostructured device configuration based on 2D materials provides a new way for future electronics and flexible electronics.

KEYWORDS

InSe, van der Waals heterostruture, 2D electronics, flexible electronics

1 Introduction

The emergence of 2D materials, such as graphene [1], transition metal dichalcogenides (TMDs) [2], black phosphorus (BP) [3], etc., as channel materials provides a promising alternative route for overcoming the scaling limits in conventional complementary metal-oxide-semiconductor devices. With 2D materials as the channel, the carriers confined to an atomically thin layer can be tuned effectively and uniformly by the gate voltage, allowing for high-operation speeds and overcoming the short-channel effects [4, 5]. Moreover, benefiting from excellent mechanical properties, 2D materials are attractive channel materials for flexible electronics compared to low-mobility organic semiconductors (typically below 10 $cm^2 \cdot V^{-1} \cdot s^{-1}$) [6] and high-cost polycrystalline silicon (mobility of ~ 50 $cm^2 \cdot V^{-1} \cdot s^{-1}$) [7]. However, the charge transport of 2D materials is sensitive to the interface between 2D-material channel and gate dielectric [8–10]. An effective approach is using atomically flat hBN with large surface optical phonon energies [11, 12] as gate dielectric to achieve high-performance electronics by effectively suppressing carrier scattering in the interface between 2D-material channel and gate dielectric [13, 14].

InSe is a layered metal-chalcogenide semiconductor that is composed of stacked layers in Se-In-In-Se atomic sequences with van der Waals interactions between layers. Due to its high electron mobility and tunable band gap, InSe is a fascinating channel material for 2D electronics [15–30] and optoelectronics [31–36]. Dielectric engineering of InSe FETs using PMMA to suppress carrier scattering from the channel-dielectric interface yielded a high room-temperature field-effect mobility of ~ 1,000 $cm^2 \cdot V^{-1} \cdot s^{-1}$, which is much better than that of TMD-based FETs (50–200 $cm^2 \cdot V^{-1} \cdot s^{-1}$) and comparable to that of BP FETs [15, 16]. Furthermore, a high-quality 2D electron gas was realized in few-layer InSe encapsulated in hBN, allowing the observation of the quantum Hall effect at low temperatures [17], indicating that such heterostructure has significant promise for high-performance electronic devices.

In this work, using an InSe/hBN/graphite heterostructure as the unit of 2D FET, with InSe as channel material, hBN as dielectric, and graphite as gate, we obtain high-performance heterostructured InSe FETs with high electron mobility up to 1,146 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at room temperature and on/off ratio up to 10^{10}. Digital inverters are constructed by integrating two such FETs with local gate modulation and an ultrahigh voltage

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gain up to 93.4 is achieved. Furthermore, the heterostructured InSe FET stacked on a flexible substrate shows little change in performance at high strain level of ~ 2%.

2 Results and discussion

Figure 1(a) presents a schematic of a 2D FET consisting of an InSe/hBN/graphite van der Waals heterostructure on a SiO_2/Si wafer, where InSe, hBN, and graphite are employed as channel material, dielectric, and gate, respectively. The InSe/hBN/graphite heterostructure stack was fabricated using mechanical exfoliation and the dry-transfer method [14, 37] in an argon atmosphere glovebox. Cr/Au (5 nm/60 nm) metal stacks were defined by standard electron-beam lithography and deposited by thermal evaporation to serve as drain and source electrodes. Detailed device fabrications are provided in Methods and Fig. S1 in the Electronic Supplementary Material (ESM). Figure 1(b) shows a false-color optical microscope of an InSe/hBN/graphite heterostructure on a SiO_2/Si wafer, where the 3.0-nm-thick graphite gate electrode is at the bottom, the 10.8-nm-thick hBN dielectric is on top of the graphite, and 15.8-nm-thick InSe channel is on top of the hBN/graphite heterostructure. The boundaries of graphite and hBN are marked by blue and white dotted lines, respectively.

The interface quality and structural features of a heterostructured InSe FET were characterized by high-angle-annual-dark-field (HAADF) imaging on an aberration corrected scanning transmission electron microscope (STEM) in the cross-section view. Figure 1(c) shows an overview HAADF-STEM image of the InSe FET in the contact region. Each layer of the device can be clearly distinguished through the atomic-number contrast in the HAADF-STEM image. Highly uniform and clean interfaces due to "self-cleansing" mechanism [38, 39] in van der Waals heterostructures can be observed between the InSe, hBN, and graphite layers. Furthermore, the Cr/Au metal stacks form direct and uniform contact with the InSe channel. The high quality of the InSe/hBN interface is further demonstrated in the atomic-resolution STEM image shown in Fig. 1(d), where an atomically sharp and uniform interface can be clearly seen between InSe and hBN without any gap or obvious defects/contamination.

Electrical characterization of such heterostructured InSe FET was carried out in vacuum at room temperature. The typical output characteristics of this InSe FET at drain-source voltage (V_{ds}) ranging from –0.1 V to +0.1 V is shown in Fig. 2(a). The good linear behavior indicates a good ohmic contact of Cr/Au electrodes at positive gate voltages (V_g). As presented in Fig. 2(b), the current exhibits a robust saturation behavior at large V_{ds}, suggesting complete capacitive coupling between the InSe channel and the hBN dielectric. The transfer characteristics at V_{ds} = 0.1 V reveals n-type conduction and a high current on/off ratio of order 10^{10} (Fig. 2(c)).

The field-effect mobility (μ_{FE}) was extracted from the linear region of the transfer curve (blue line in Fig. 2(c)) using the following equation

$$\mu_{FE} = \frac{L}{W}\frac{1}{C_i}\frac{1}{V_{ds}}\frac{dI_{ds}}{dV_g} \quad (1)$$

where L is the effective channel length of 30 μm, W is the effective channel width of 10.3 μm, C_i is the capacitance of 10.8-nm-thick hBN dielectric of 3.28×10^{-7} F·cm^{-2}, and V_{ds} is the drain-source voltage of 0.1 V. The calculated μ_{FE} of this heterostructured InSe FET is 1,146 cm^2·V^{-1}·s^{-1}, which is one order of magnitude higher than the value of 122 cm^2·V^{-1}·s^{-1} of the InSe FET on a SiO_2/Si substrate with InSe, 300 nm SiO_2, and p^{++} silicon as channel material, dielectric, and gate, respectively (Fig. S2 in the ESM). This high mobility indicates the effective suppression of carrier scattering from the dielectric substrate. The great improvement in mobility is due to the atomically flat hBN and compatible interface between InSe and hBN.

The subthreshold swing (SS) was estimated from the transfer curve in logarithmic scale (black line in Fig. 2(c)) using the following equation

$$SS = dV_g/d(\log I_{ds}) \quad (2)$$

The calculated SS of this heterostructured InSe FET is 0.372 V·dec^{-1}, which is much lower than the value of 6.09 V/dec of InSe FETs on a SiO_2/Si substrate (Fig. S2 in the ESM). On the one hand, the effective reduction of SS is due to the larger capacitance of the 10.8-nm-thick hBN dielectric compared to that of 300-nm-thick SiO_2 dielectric. On the other hand, the

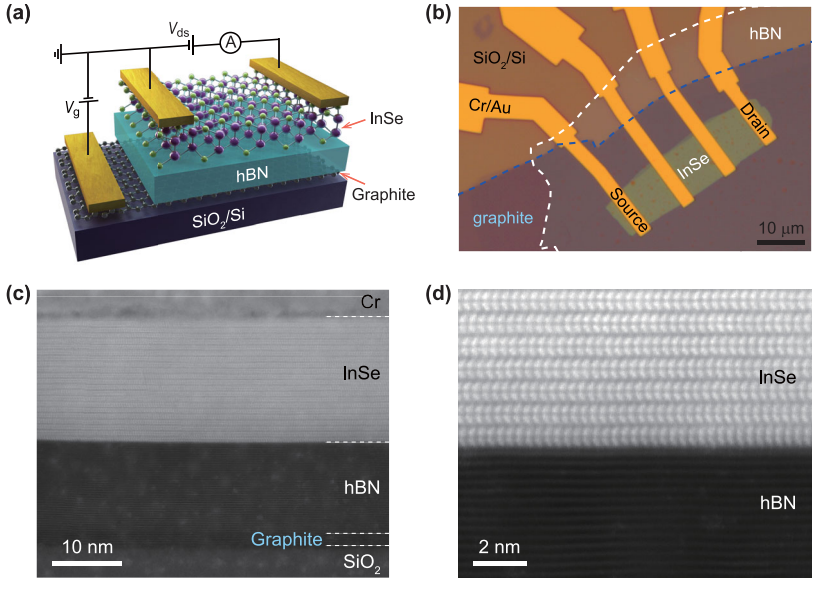

Figure 1 2D FET based on InSe/hBN/graphite van der Waals heterostructure. ((a) and (b)) Schematic and optical microscope of a heterostructured InSe FET with Cr/Au as contact electrodes on a SiO_2/Si wafer, where InSe, hBN, and graphite are employed as channel material, dielectric, and gate, respectively. (c) An overview HAADF-STEM cross-section of the InSe FET at contact region. The white dotted lines show interfaces of different layers. (d) Atomic-resolution HAADF-STEM of InSe/hBN interface.

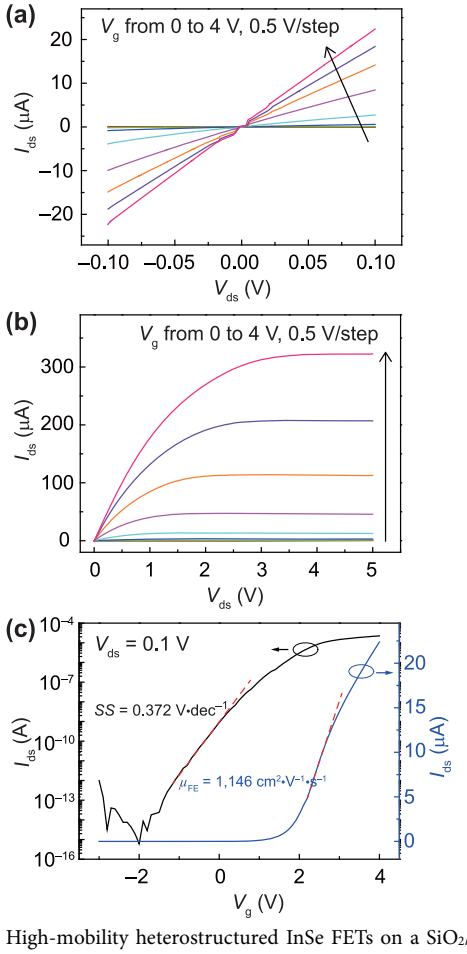

Figure 2 High-mobility heterostructured InSe FETs on a SiO_2/Si wafer. ((a) and (b)) Output characteristics of the heterostructured InSe FET at small V_{ds} range from −0.1 V to 0.1 V, and large V_{ds} range from 0 to 5 V. The gate is from 0 to 4 V with a step of 0.5 V. (c) Transfer characteristics of the heterostructured InSe FET at V_{ds} = 0.1 V in linear (blue line) and logarithmic (black line) scales. The two red dotted lines are linearly fitted in the linear region of blue line and in the subthreshold region of black line to extract μ_{FE} of 1,146 cm^2·V^{-1}·s^{-1} and SS of 0.372 V·dec^{-1}, respectively.

interfacial density of trapped charge is known to be smaller in InSe/hBN compared to that in InSe/SiO_2 interfaces [40] and is, therefore, another factor for the improvement of the SS of the present heterostructured InSe FETs. To demonstrate that the high performance of the heterostructured InSe FETs with high mobility and relatively low SS does not vary significantly from device to device, transfer curves of two additional devices are shown in Fig. S3 in the ESM. The on/off ratio are both 10^{10}. The mobilities are 1,161, 1,149 cm^2·V^{-1}·s^{-1}, and the SS values are 0.52, 0.277 V·dec^{-1}, respectively, further confirming the high quality of the interface between hBN and InSe.

However, the SS is still large compared to the ideal value of 60 mV·dec^{-1}. Using the same device configuration with a few-layer-MoS_2/hBN/graphite heterostructure on a SiO_2/Si wafer, the measured SS is 76.4 mV·dec^{-1} (Fig. S4 in the ESM), close to that of the ideal value. The room-temperature field-effect mobility and on/off ratio of the MoS_2 FET are 40 cm^2·V^{-1}·s^{-1} and 10^9, respectively. The large SS of InSe FET may be attributed to the large depletion capacitance of InSe or large contact resistance at the subthreshold region. The contact resistance of a heterostructured InSe FET with Cr/Au stack as contact electrodes decreases with increasing graphite gate voltage (Fig. S5 in the ESM). Using graphite as contact electrodes, the electron mobility is 605 cm^2·V^{-1}·s^{-1} and the SS value is improved to 132 mV·dec^{-1} (Fig. S6 in the ESM). In addition, InSe is less stable than MoS_2 [17], which may cause light degradation of InSe during device fabrication and hence higher trapped-charge density in InSe/hBN as compared with that in MoS_2/hBN, resulting in a larger SS. To further improve the SS, contact and interfacial engineering is needed in future work.

The high-performance 2D InSe FETs based on InSe/hBN/graphite heterostructure with high mobility and relatively low SS has major implications in constructing 2D logic circuits, in which a digital inverter is an important elemental device. As a simple example, a prototype 2D digital inverter can be constructed by integrating two InSe FETs, as schematically shown in Fig. 3(a). Figure 3(b) shows a false-color optical microscope of a heterostructured InSe inverter. Two separate graphite flakes are used as the local gate electrodes and Cr/Au stacks are used as the contact electrodes to the InSe channel. The boundaries of graphite and hBN are marked by blue and white dotted lines, respectively. A detailed device-fabrication flow chart is shown in Fig. S7 in the ESM. Figure 3(c) shows the output voltage (V_{out}) as a function of input voltage (V_{in}) when the

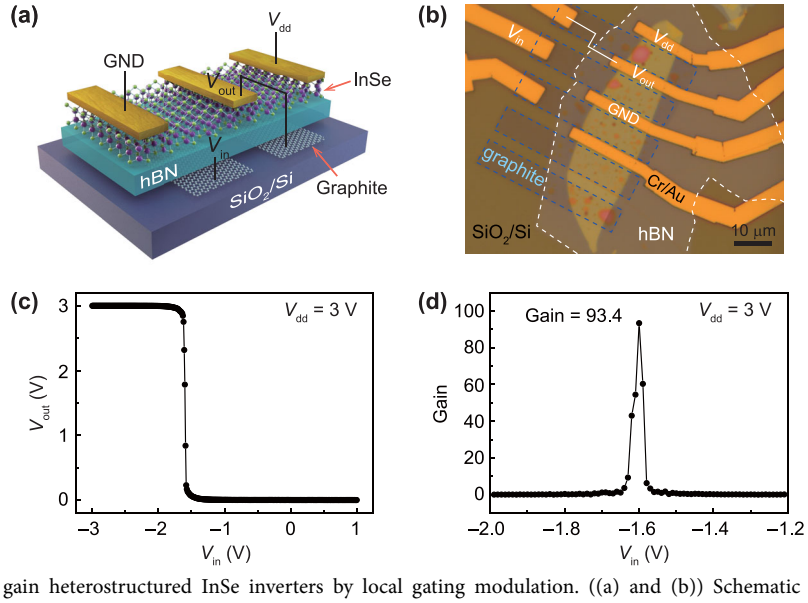

Figure 3 Ultrahigh voltage gain heterostructured InSe inverters by local gating modulation. ((a) and (b)) Schematic and optical microscope of a heterostructured InSe inverter constructed by integrating two InSe FETs on a SiO_2/Si wafer. (c) V_{out} as a function of V_{in} of the InSe inverter at V_{dd} = 3 V. (d) Voltage gain as a function of V_{in}. The peak voltage gain of the InSe inverter is up to 93.4 at V_{dd} = 3 V.

supply voltage (V_{dd}) is 3 V, where V_{dd} is applied to one of the outer contact electrodes with the other outer contact electrode grounded, V_{in} is applied to one of the local graphite gate electrodes close to the grounded contact electrode, and V_{out} is measured between the other local graphite gate electrode and the middle contact electrode. V_{out} shows three different regimes with two different logic states. When V_{in} is above −1.5 V, V_{out} is approaching 0 V, which can be denoted as digital 0. Oppositely, when V_{in} is lower than −2 V, V_{out} is approaching V_{dd} (3 V), which can be denoted as digital 1. The output swing (defined as the largest variation of V_{out}) is quite close to V_{dd}, indicating the high inverting capability of this inverter.

A key figure of merit of the inverter is the voltage gain, which is defined as $-dV_{out}/dV_{in}$, and indicates the sensitivity of V_{out} in response to the change in V_{in}. An ultrahigh voltage gain of up to 93.4 of this InSe inverter at V_{dd} = 3 V is shown in Fig. 3(d). Even when V_{dd} is 2 V, the voltage gain can still reach 82.1 (Fig. S8 in the ESM). This voltage gain is ultrahigh compared to that of other inverters based on 2D materials [41–51] (Table S1 in the ESM), with only one exception, WSe_2-MoS_2 complementary inverter (voltage gain reaches 110 at V_{dd} = 2 V) [50]. The voltage gain of the present inverters is much larger than the unity gain (gain = 1) required in integrated circuits composed of multiple cascade inverters, indicating their potential in digital-inverter applications.

Furthermore, taking advantage of the well-known mechanical flexibility of 2D materials, an InSe/hBN/graphite heterostructure was stacked on flexible substrates to examine the performance of InSe flexible electronics. Figure 4(a) shows a schematic of a heterostructured InSe FET on a flexible substrate (125-μm-thick polyethylene naphthalate (PEN)). Detailed device fabrication is provided in the Experimental Section. Electrical characterization was measured under atmospheric environment and different bending conditions at room temperature. The fabricated InSe FET (19.8-nm-thick InSe, 14.6-nm-thick hBN, 14-nm-thick graphite) also exhibits high field-effect mobility of 536 $cm^2V^{-1}·s^{-1}$ without bending (Fig. 4(b)). The high-mobility heterostructured InSe FET is independent of supported flexible substrate because the mobility of the InSe FET is mainly determined by the interface of InSe/hBN. We observed that there is just a weak change in transfer curves at large strain conditions (Fig 4(b)). Figure 4(c) presents the relative electron mobility of μ/μ_0 as function of strain, where μ_0 is the mobility without bending. The inset shows a photograph of the InSe FET on a PEN substrate under test at 2% strain condition. There is only a 6.5% mobility decrease at large strain up to 2% due to the great mechanical flexibility of InSe, hBN, and graphite.

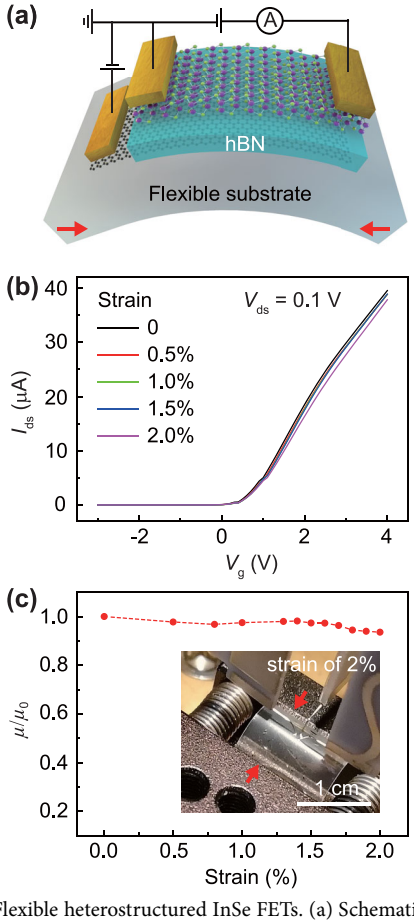

Figure 4 Flexible heterostructured InSe FETs. (a) Schematic of a heterostructured InSe FET with Cr/Au as contact electrodes on a flexible substrate. (b) Transfer curves of the InSe FET at V_{ds} = 0.1 V under different bending conditions up to 2% strain. (c) Relative electron mobility μ_0/μ as a function of strain. The inset presents photograph of the InSe FET on a PEN substrate under test at 2% strain.

3 Conclusions

In conclusion, based on InSe/hBN/graphite heterostructure, high-performance 2D electronics and flexible electronics are easily obtained. The heterostructured InSe FETs show high electron mobility of 1,146 $cm^2·V^{-1}·s^{-1}$, high on/off ratio of 10^{10}, and relatively low SS of 0.372 $V·dec^{-1}$. By integrating such InSe FETs with separate graphite local gates, the resulting inverter shows an ultrahigh voltage gain up to 93.4, which is ultrahigh among inverters based on 2D materials. Moreover, heterostructured InSe FETs integrated on the flexible substrate exhibits excellent and stable performance even at 2% strain. Therefore, this heterostructured device based on 2D materials is a promising device configuration for future electronics and flexible electronics if high-quality wafer-scaled channel materials and hBN gate dielectric can be obtained.

4 Methods

4.1 Device fabrication and characterization

Bulk InSe, hBN, and graphite crystals were purchased from 2D semiconductors, HQ graphene, and NGS Naturgraphit companies, respectively. The InSe/hBN/graphite heterostructures were prepared using mechanical exfoliation and dry-transfer method. First, graphite flakes were mechanically exfoliated onto a silicon wafer pre-processed by oxygen plasma. Then the silicon wafer with graphite flakes was annealed in flowing 100 sccm H_2/Ar gas at 400 °C for 3 hours. Then a mechanically exfoliated hBN flake on PDMS was stacked on top of the target graphite flake by the dry-transfer method. Then the silicon wafer with hBN/graphite heterostructure was annealed in flowing gas at 400 °C for 3 h again. Finally, the mechanically exfoliated InSe flake on PDMS was stacked on top of hBN/graphite heterostructure. For the InSe/hBN/graphite heterostructure on a PEN substrate, the same process was employed except for the annealing steps. The heterostructured InSe FETs and inverters on silicon wafers were protected by a spin-coated PMMA layer immediately after lift-off. The heterostructured InSe FETs on PEN substrates were protected by stacking a hBN flake immediately after lift-off. Electrical characterization was carried out using a Keithley 4200 semiconductor characterization system and a Janis probe station. The thickness of InSe, h-BN, and graphite flakes were determined by a Bruker Dimension Edge atomic force microscope after electrical measurments.

4.2 STEM sample preparation and characterization

Before STEM sample fabrication, the heterostructured InSe

FET was protected by covering it with a graphite flake using the dry-transfer method. For high-resolution imaging, a cross sectional TEM lift-out sample was fabricated using an FEI Helios NanoLab G3 CX focused ion beam microscope. The HAADF imaging was performed using an aberration-corrected Nion HERMES-100 STEM at 60 kV. All images were obtained using an illumination semi-angle of 32 mrad with the collection semi-angle from 75 to 210 mrad.

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Electronic Supplementary Materials: Supplementary material (InSe FET on a SiO_2/Si substrate, additional heterostructured InSe FETs, low-SS heterostructured few-layer MoS_2 FET, contact resistance of a heterostructured InSe FET, low-SS heterostructured InSe FETs with graphite as contact electrodes, test for the inverter at V_{dd} = 2 V, comparison of voltage gain of integrated digital inverters based on 2D materials) is available in the online version of this article at http://doi.org/10.1007/s12274-020-2757-1.

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