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Processing of an atomically smooth Ge(001) surface on a large scale

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Abstract
An atomically smooth Ge(001) surface on a large scale is obtained by deposition of submonolayer Ge on a Ge(001) surface at 300 °C, which repairs the missing dimer defects produced during the enhanced energy ion bombardment and annealing of the substrate. The Ge(001) samples are characterized by scanning tunnelling microscopy (STM) before and after the submonolayer Ge deposition. The ion bombardment/subsequent annealing processing and STM tip induced defects are also investigated in detail.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Recently, the Ge(001) surface has attracted much attention because of its great importance in the semiconductor materials industry [1–4]. It has been reported that if Ge is incorporated in Si structures, the mobility of the Si layers can be greatly enhanced [5]. Therefore, a lot of investigations have focused on the homoepitaxial growth of Ge(001) in an effort to understand the epitaxial growth of Ge on Si(001) in detail [6–12]. Among these investigations, fabrication of an almost defect free Ge surface on a large scale becomes more and more important, because this would possess good properties for Si/Ge heterojunction device use and for investigation of the adsorption or diffusion process of foreign atoms on it. A repeated ion bombardment/annealing method is commonly used for fabricating the Ge surface because of the low melting point of germanium (937 °C) [13–15]. Using this method, with a lightly doped Ge(001) sample, Zandvliet *et al* fabricated an ordered domain pattern consisting of c(4 × 2) and 2 × 1 strips [16]. For highly doped Ge samples, it is easier for the doped elements to come to surface of the sample during the treatment process. Enhanced energy ion bombardment can be used to remove them; however, it causes defect damages simultaneously. This damages cannot be completely repaired by a subsequent annealing process, so different surface fabrication techniques have been reported for preparation of clean Ge surfaces [17–19]. Among them, growth of a thick Ge buffer layer after ion bombardment/annealing is an effective method [19]. All in all, the preparation of large scale almost defect free Ge(001) surfaces suitable for investigations is still a challenge.

In this work, we put forward a new method, rather than growth of a thick Ge buffer layer, for fabricating a clean Ge surface. There are defects with 12% concentration on the Ge surface after the ion bombardment/annealing treatment process; these defects can be repaired by submonolayer Ge deposition at a substrate temperature of 300 °C. Using this method, large scale and atomically smooth Ge(001) surfaces can be obtained repeatedly. The surfaces obtained are analysed by room temperature STM and using low energy electron diffraction (LEED).

2. Experimental details

All experiments were carried out in an ultrahigh vacuum (UHV) system with a base pressure of 6×10^{-11} Torr, which contains two UHV chambers, a preparation chamber and an analysis chamber. The former chamber is equipped with an argon ion sputtering gun for cleaning the germanium surface and evaporators with integral flux monitors (EFM) for depositing Ge atoms on it. The latter consists of a room temperature STM (Omicron STM 1 with SCALA electronics) and a LEED optics system.

A germanium sample with a size of 12 × 5 mm^2 on a Mo sample stage was cut from an n-type highly Sb doped Ge(001) wafer (RT resistivity: <0.1 Ω cm, 0.3 mm thick,

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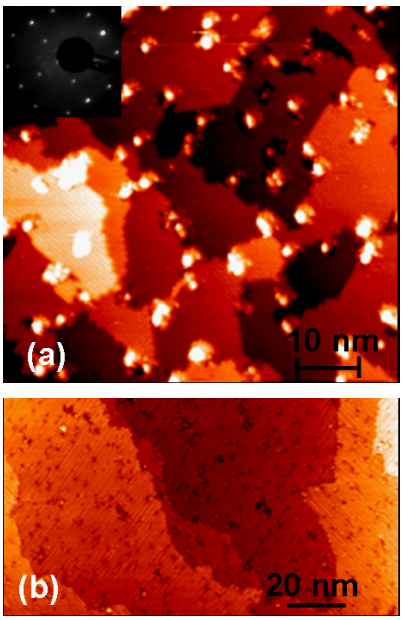

Figure 1. (a) STM image of a Ge(001) surface obtained by two ion bombardment/annealing cycles on a new sample. Scanning size: 66×66 nm^2. The image was recorded at room temperature with $V_{\text{bias}} = +1.86$ V and $I_t = 0.20$ nA. The inset shows the LEED pattern (130 eV) observed at room temperature. (b) The large scale STM images of the Ge(001) surface obtained by enhancing the energy of the ion bombardment and with six cleaning cycles. Scanning size: 134×75 nm^2. Sample bias voltage: $+1.00$ V; tunnelling current: 0.37 nA.

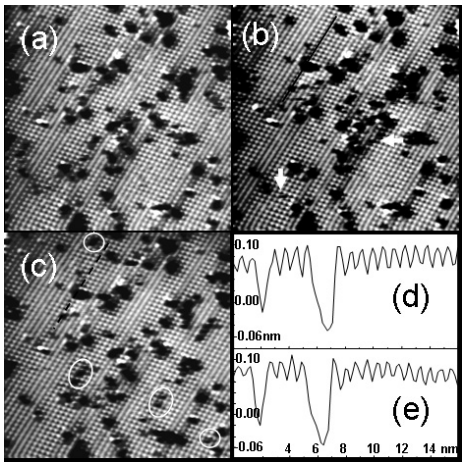

Figure 2. ((a)–(c)) Close-up STM images of the Ge(001) surface obtained, shown in figure 1(b). They are successively obtained for the same area (37×37 nm^2) with different tunnelling currents at room temperature. ((a), (b)) Tunnelling current 0.24 nA and sample bias voltage 2.20 V. (c) Tunnelling current 0.34 nA and sample bias voltage 2.20 V. ((d), (e)) The line profiles present the tip displacement as a function of position along the solid and dashed lines indicated in (b) and (c), respectively, revealing that the defects are in the top layer of the Ge(001) surface.

one-side polished). The Ge sample was pre-cleaned through a strict process before it was inserted into the UHV chamber via a load-lock chamber and then degassed completely by direct current (DC) heating in the preparation chamber. We cleaned the Ge substrate by means of Ar ion bombardment at room temperature and then annealed it while keeping the vacuum in the 10^{-10} Torr range. During the exposure of the sample to the ion beam, the background pressure in the preparation chamber is 1.7×10^{-5} Torr. The distance between the outlet of the sputtering gun and the substrate is about 125 mm, and the Ar ion beam is incident on the sample at an angle of 20° from the substrate normal direction. Then we deposited about 0.10 ML (1 ML is the amount of Ge needed to saturate the substrate only with 2D islands) of Ge at 300 °C on the Ge(001) surface obtained, using an evaporator with an integral flux monitor which can precisely control the amount of deposition. The temperature was determined using an infrared thermometer. Electrochemically etched W tips were used to obtain all the STM observations of the processed Ge(001) samples at room temperature and a bias voltage was applied to the sample in this work, so that positive biases probe the unoccupied states of the sample.

3. Results and discussion

The topography obtained by the STM at room temperature after two ion bombardment/annealing cycles of a new Ge(001) substrate is shown in figure 1(a). Every time, the ion bombardment spans for 10 min at a flux of 4.6 μA cm^{-2}. The annealing process is at 800 ± 20 °C for 10 min. On the surface, many protrusions are observed, which are probably due to contaminations such as C [19] and the dopant elements Sb, due to their migration from bulk to the surface during annealing, which is especially easy for the highly doped Ge sample. In figure 1(a), most of the protrusions are located at the steps, and some stay near the vacancy defects on the terraces. The structure of the Ge(001) surface obtained was determined from the LEED pattern as shown in the inset of figure 1(a), which was obtained at room temperature.

A Ge(001) surface with protrusions cannot be used as a substrate for investigation of the process of adsorption of foreign atoms on it because the protrusions may act as nucleation sites and may impede the adsorption mechanism. These protrusions, shown in figure 1(a), can be thoroughly eliminated on a large scale, as shown in figure 1(b), by enhancing the energy of the ion bombardment with the flux increasing to 5.7 μA cm^{-2} and increasing the number of cleaning cycles to six. For one cycle, the ion bombardment spans 12 min and the annealing is at 800 ± 20 °C for 10 min. Missing dimer defects are randomly distributed on the surface. Statistically, the concentration of these defects is about 12%. In addition, symmetric dimers (2×1) as well as buckled dimers ($c(4 \times 2)$) can be distinguished in the subsequent images, as shown in figure 2. Figures 2(a) and (b) are obtained with the same tunnelling conditions. Between the two images, the time lapse is about 25 min and another four images are obtained, which are same and not shown here. As reported by Zandvliet *et al*, under tunnelling conditions of 1 nA, and a negative sample bias of 1.5–2.0 V, Ge ad-dimers and small Ge clusters can be removed from the substrate by the STM tip, so missing dimer defects are newly created on Ge(001) or annihilated at room temperature [20]. As in our case, during a longer scanning time (25 min) and under the tunnelling conditions of 0.24 nA, 2.20 V, no missing dimer defects disappear or are

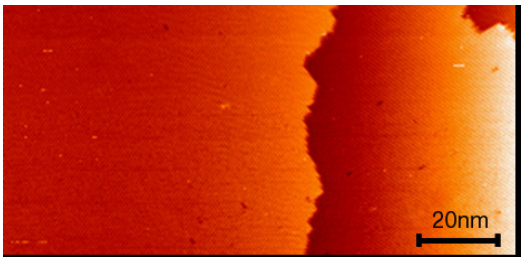

Figure 3. Filled state STM image of a large scale (132×64 nm^2) almost defect free Ge(001) surface obtained by many enhanced energy ion bombardment/annealing cycles, and a subsequent submonolayer Ge deposition method. The tunnelling current is 0.36 nA and the sample bias voltage is -1.47 V.

newly formed. These defects, shown in the figures 2(a) and (b), could be thought to be formed during the previous treatment process. Kyuno *et al* [21] reported that He ion bombardment of Si(001) yielded surface defects and bulk defect migration to the surface. Missing dimer vacancies on Si(001) created by ion bombardment have been reported in many references [22–25]. Kim and co-workers [26] also reported surface defects created by 20 keV Xe ion irradiation on Ge(111). Feil *et al* [23] reported that the buried vacancies could migrate to the surface of Si during the annealing process. So it is possible that the surface missing dimer defects shown in figures 2(a) and (b) are produced directly by enhancing the energy of the ion bombardment and by the migration of buried vacancies to surface during the treatment process.

When the tunnelling current increases from 0.24 to 0.34 nA, some missing dimer defects are newly created on the surface and these are labelled with ellipses in figure 2(c). The interaction between the substrate and the atoms at the very edge of the W tip could modify the surface morphology. When the tunnelling current increases, the interaction between the tip and the substrate increases. During scanning, some dimers are removed from their original position and picked up by the STM W tip, which could refill existing missing dimer defects, indicated by white arrows in figure 2(b) [20].

The line profiles shown in figures 2(d) and (e) present the tip displacement as a function of position along the solid and dashed lines indicated in figures 2(b) and (c), which span across missing dimer defects. The line profiles show that the missing dimer defects have a depth of 0.13 ± 0.01 nm, which is about a monatomic layer height, indicating that the defects are in the top layer of the Ge(001) surface.

Figure 3 shows the STM image of a large scale atomically smooth Ge(001) surface obtained after submonolayer deposition. The fact that during scanning the dimers picked up by the W tip could detach and repair the missing dimer defects implies that these defects are energetically more favourable positions. The deposited germanium atoms have a surface diffusion coefficient D ($D \propto \exp(-V_s/kT)$, where V_s is the potential energy barrier, from site to site, k is the Boltzmann constant and T is the substrate temperature) [27]. They can easily move to and reside on the positions of missing dimer defects, and form a reconstruction which is similar to the surrounding construction. Although the surface obtained still contains several defect dents, as shown in figure 3, it is suited for epitaxial growth investigations as a substrate.

4. Conclusions

In summary, the defects induced by ion bombardment/annealing and the STM tip during subsequent scanning are discussed in detail and have about 12% concentration. An almost defect free Ge(001) surface on a large scale is fabricated by depositing about 0.10 ML of Ge at 300 °C on the substrate obtained. With this method, such a clean Ge(001) surface can be repeatedly fabricated, especially for highly doped Ge samples. This processing will be helpful for future Ge based electronics and for epitaxial growth of the Si/Ge and/or other systems.

Acknowledgments

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